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Enhancement of Voltage Quality in Isolated Power Systems

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ABSTRACT

A traditional method to achieve improved power quality (PQ) is to use passive filters connected at the sensitive load terminals. However, this practice has some shortcomings: the effectiveness of the scheme could deteriorate as the source impedance or load condition changes; it can lead to resonance between the filter and the source impedance.
In this paper the use of series compensators (SCs) in improving voltage quality of isolated power systems is considered. The roles of the compensators are to mitigate the effects of momentary voltage sags/swells and to control the level of harmonic distortions in the networks. SC injects harmonic currents of the same magnitude but of opposite polarity to cancel the harmonics present there. A control strategy for the SC is developed to regulate power flow. This is achieved through phase adjustment of load terminal voltage. It leads to an increase in the ride through capability of loads to the voltage sags/swells. The isolated power systems are often considered weak in that they possess relatively lower short-circuit ratio, in comparison to a grid. Network voltage control becomes a challenging task as a result. The power quality problem is compounded with the drive-converter load. The sensitive loads would be connected in parallel with the nonlinear drive. Often such sensitive loads also contain input rectifiers that are capacitive in nature. The total capacity of the sensitive loads could be much smaller than that of the main drives; the distorted supply voltage is harmful to the sensitive loads. Excessive voltage distortions could cause the sensitive loads to maloperate. The loads are also sensitive to short-duration disturbances, in the form of voltage sags or swells.
Validity of the proposed technique is illustrated through simulation. Simulation has confirmed the effectiveness of the proposed method, as it is applied on the SC to achieve improved quality of supply in the power system.

Key words: Voltage quality, power quality, series compensator, voltage sags/swells

1. INTRODUCTION

The typical definition for a harmonic is "a sinusoidal component of a periodic wave or quantity having a frequency that is an integral multiple of the fundamental frequency. Some references [1to2] refer to "clean" or "pure" power as those without any harmonics. Harmonics have been around for a long time and will continue to do so[3to5]with effects like:

- Overheated transformers, especially delta windings where triplen harmonics generated on the load side of a delta-wye transformer will circulate in the primary side.
- Nuisance operation of protective devices, including false tripping of relays and failure of a UPS to transfer properly, especially if controls incorporate zero-crossing sensing circuits.
- Bearing failure from shaft currents through uninsulated bearings of electric motors.
- Blown-fuses on PF correction caps, due to high voltage and currents from resonance with line impedance.
- Mis-operation or failure of electronic equipment
- If there are voltage subharmonics in the range of 1-30Hz, the effect on lighting is called flicker. This is especially true at 8.8Hz, where the human eye is most sensitive, and just 0.5% variation in the voltage is noticeable with some types of lighting.

The switching-type power supplies found in most personal computers and peripheral equipment, such as printers,while they offer many benefits in size, weight and cost, the large increase of this type of equipment over the years is largely responsible for the increased attention to harmonics.

Rectifiers convert AC voltage into DC voltage, which is further converted into other voltages that the equipment needs to run. The rectifier consists of semi-conductor devices (such as diodes) that only conduct current in one direction. In order to do so, the voltage on the one end must be greater than the other end. These devices feed current into a capacitor[6], where the voltage value on the capacitor at any time depends on how much energy[7] is being taken out by the rest of the power supply.

Harmonic filters[8] are used to eliminate the harmonic distortion caused by nonlinear loads. Specifically, harmonic filters are designed to attenuate or in some filters eliminate the potentially dangerous effects of harmonic currents active within the power distribution system. Filters[9]can be designed to trap these currents and, through the use of a series of capacitors, coils, and resistors, shunt them to ground. A filter may contain

several of these elements, each designed to compensate a particular frequency or an array of frequencies.

2. HARMONIC MITIGATION AND POWER FLOW IN ISOLATED POWER SYSTEM

With regard to the problem in hand, it is assumed that the nonlinear converter and the sensitive loads are balanced. In what follows, symbols with the subscript "S" denote quantities which are associated with the upstream source, "L" for those associated with the sensitive load, "D" with the downstream main converter drive and "C" with the series compensator. Subscript "H" denotes the **h**th harmonic component and "1" that of the fundamental. Voltage and current Phasor are denoted with a symbol "$\rightarrow$" on the top of the respective quantities. Their magnitudes (rms) are shown as capital letters while their peak values are denoted with "$\wedge$" on top. Vectors are denoted by bold letters. As shown in Fig. 1, the central part of the SC is the voltage source inverter (VSI) and the energy storage system (ESS). As PWM switching scheme is often used in the VSI, harmonics are generated and filtering is required. L_f and C_f are the filter inductance and capacitance. The VSI synthesizes the required voltage quantity which would be injected in series with V_L. The ESS would act as a buffer and provides the energy needed for load ride through during a voltage-sag. Conversely, during a voltage-swell, excess energy from the network would be stored in the ESS so that V_L can be controlled.

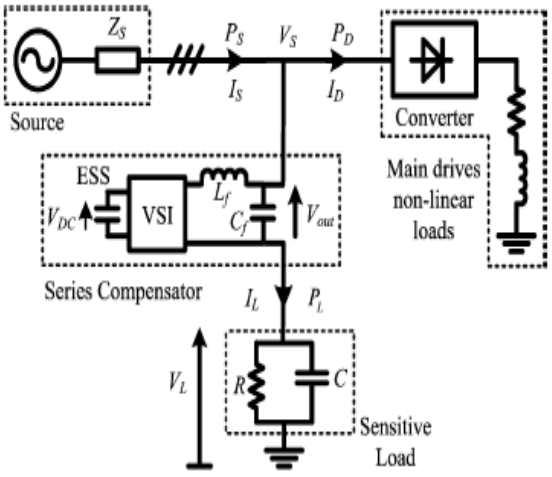


Fig.1. Typical isolated power system installed with an SC.

2.1 Control of Harmonic Distortions

Distorted phase voltage Vs on the upstream source-side of the sensitive load can be expressed as shown in (1) at the bottom of the page for phases a, b, and c where ω_o is the fundamental frequency, n is the harmonic order; V_{on} is the zero phase sequence voltage component; V_{1n} and φ_{1n} are the peak and phase of the positive phase sequence voltage component; V_{2n} and φ_{2n} are the peak and phase of the negative phase sequence voltage component. When expressed in this manner, V_s would be completely general and would include unbalances in the network. Clearly, distorted voltage is undesirable at the sensitive load terminals. The fundamental components of the voltages contained in (1) are

$$\boldsymbol{V}_S = \begin{bmatrix} \boldsymbol{V}_{Sa} \\ \boldsymbol{V}_{Sb} \\ \boldsymbol{V}_{Sc} \end{bmatrix} = \begin{bmatrix} \sum_{n=1}^{\infty}[V_{0n} + \hat{V}_{1n}\sin(n\omega_o t + \varphi_{1n}) + \hat{V}_{2n}\sin(n\omega_o t + \varphi_{2n})] \\ \sum_{n=1}^{\infty}[V_{0n} + \hat{V}_{1n}\sin(n\omega_o t + \varphi_{1n} - 2n\pi/3) \\ \qquad + \hat{V}_{2n}\sin(n\omega_o t + \varphi_{2n} + 2n\pi/3)] \\ \sum_{n=1}^{\infty}[V_{0n} + \hat{V}_{1n}\sin(n\omega_o t + \varphi_{n} + 2n\pi/3) \\ \qquad + \hat{V}_{2n}\sin(n\omega_o t + \varphi_{2n} - 2n\pi/3)] \end{bmatrix}$$

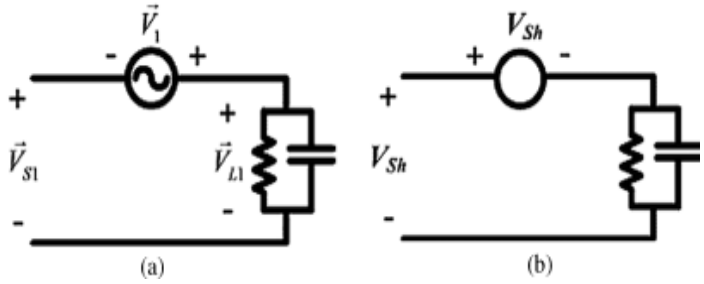


Fig. 2: Equivalent circuits of the sensitive load-SC branch for (a) fundamental component and (b) hth harmonic component.

$$\boldsymbol{V}_{S1} = \begin{bmatrix} V_{Sa1} \\ V_{Sb1} \\ V_{Sc1} \end{bmatrix} = \begin{bmatrix} \hat{V}_{11}\sin(\omega_o t + \varphi_{11}) \\ \hat{V}_{11}\sin(\omega_o t + \varphi_{11} - 2\pi/3) \\ \hat{V}_{11}\sin(\omega_o t + \varphi_{11} + 2\pi/3) \end{bmatrix}. \quad (2)$$

From (1) and (2), therefore

$$V_S = \boldsymbol{V}_{S1} + \boldsymbol{V}_{Sh} \quad (3)$$

Where $\mathbf{V}_{sh}$ contains all the harmonic components in (1). The proposed voltage injection method is to inject voltage components in series with $\mathbf{V}_s$ and the desirable injected voltages would contain all the harmonic components in (1). Hence, from (1) and (2), the injected voltage from the SC would be:

$$\mathbf{V}\text{out} = -\mathbf{V}\text{sh} = \mathbf{V}\text{s1} - \mathbf{V}\text{s}.$$

Thus far, one has only considered the condition that $\mathbf{V}_s$ contains harmonic distortions. However, a voltage

sag/swell may appear in $\mathbf{V}_s$ and $\mathbf{V}_{s1}$ hence, could differ from specified desirable value. Assume the desirable load side fundamental voltage components are extracting the fundamental component of Vout and denoting it by the Phasor $\mathbf{V}_1$, one obtains:

$$\vec{V}_1 = \vec{V}_{L1} - \vec{V}_{S1}. \qquad (7)$$

In this way, the equivalent circuit describing the sensitive load branch can then be decomposed into the fundamental frequency component and harmonic component circuits, as shown in Fig. 2(a) and (b), respectively. Under such an ideal compensation situation, there will be no harmonic component in the sensitive load current I_L and thus, no harmonic energy exchange can exist between the SC and the external system. Energy exchange is only due to the fundamental frequency components of $\mathbf{V}_{out}$ and $\mathbf{I}_L$. In practice, however, the SC has a finite bandwidth. A phase lag inevitably exists between Vsh and the actual injected voltage $\mathbf{V'}_{sh}$ from the SC. The lag results in voltage pulses appearing at the terminals of the sensitive load.

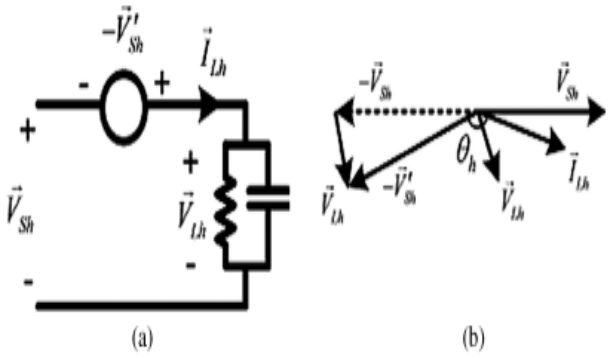


Fig. 3: Sensitive load-SC branch (a) Equivalent circuit describing harmonic compensation and (b) phasor diagram for h[th] harmonic order.

As the RC sensitive load impedance decreases with frequency, the voltage pulses will cause large harmonic current distortions to appear in I_L. A practical method to limit the THD in I_L to a prespecified level has been proposed in. It involves a new strategy to control Vout and the use of a series filter. Essentially, V_{out} is obtained from **I**L, through a lead-lag feedback scheme while the series filter reduces high-frequency harmonics in $\mathbf{I}_L$. Hence, there will be harmonic current **I**Lh in the circuit, as shown in Fig. 3(a). As $\mathbf{V'}_{sh}$ contains harmonic components, harmonic power flow can exist between the SC and the external system.

2.2 Power Flow Control through SC

Having described the harmonic mitigation principle and noting that harmonic power flow would exist in the SC circuit, detailed analysis will be carried out next. For the convenience of analysis and assuming negligible unbalances in the network, a single-phase equivalent system (phase "a") is used to describe the three-phase system shown in Fig. 1. Let the fundamental frequency component of the sensitive load current $\mathbf{I}_{L1}$, be taken as the reference Phasor. In general, the instantaneous SC output power is given by

$$p_C(t) = V_{\text{out}}(t) I_L(t). \qquad (8)$$

Suppose the upstream load change has resulted in momentary sags/swells in $\mathbf{V}_{s1}$. The aim of the compensation is to ensure the magnitude of is maintained constant. If one were to introduce a phase-shift α into $\mathbf{V}_{L1}$, one would obtain a new injection voltage from that described by (6), i.e.,

$$V_{\text{out}}(t) = \hat{V}_{L1}\sin(\omega_o t + \varphi_{11} + \alpha) - [V_{S1}(t) + V'_{Sh}(t)]. \quad (9)$$

In this way

$$\begin{aligned} p_C(t) &= V_{\text{out}}(t) I_L(t) \\ &= \left[\hat{V}_{L1}\sin(\omega_o t + \varphi_{11} + \alpha) - \hat{V}_{11}\sin(\omega_o t + \varphi_{11}) \right. \\ &\quad \left. - \sum_{h=2}^{\infty} \hat{V'}_{Sh}\sin(h\omega_o t + \varphi'_h)\right] \\ &\quad \cdot \left[\hat{I}_{L1}\sin(\omega_o t) + \sum_{h=2}^{\infty} \hat{I}_{Lh}\sin(h\omega_o t + \sigma_h)\right] \end{aligned} \qquad (10)$$

where h is harmonic order $\mathbf{V'}_{sh}$ and $\boldsymbol{\varphi}'_{sh}$ are the peak value and phase of the harmonic component of the actual injection voltage; $\mathbf{I}_{Lh}$ and $\boldsymbol{\sigma}_h$ are the peak value and phase of the hth harmonic component in $\mathbf{I}_L$. The cycle-average value of **P**c(t) is seen to contain two terms: a contribution each from the fundamental frequency component and the harmonics.

$$\mathbf{P}c = \mathbf{P}c1 + \mathbf{P}ch$$

$$P_{C1} = \tfrac{1}{2}\hat{V}_{L1}\hat{I}_{L1}\cos(\varphi_{11} + \alpha) - \tfrac{1}{2}\hat{V}_{11}\hat{I}_{L1}\cos(\varphi_{11})$$

$$P_{Ch} = -\tfrac{1}{2}\sum_{h=2}^{\infty}\hat{V'}_{Sh}\hat{I}_{Lh}\cos(\theta_h) \text{ where } \theta_h = \varphi'_h - \sigma_h$$

Where $\mathbf{P}_{c1}$ corresponds to the power flow of the fundamental frequency component. It is controllable through the introduced phase shift α in $\mathbf{V}_{L1}$. Thus, P_c can be varied through Pc1 via adjustments in α. $\mathbf{P}_{ch}$. Corresponds to the power flow of the harmonic components. In the process of varying $\mathbf{P}_{c1}$, $\mathbf{P}_{ch}$ is assumed constant over the time interval when α is being adjusted. This is a reasonable assumption because the adjustments in

α can be accomplished in a much shorter time, as the rate by which the electro-mechanical drive load and therefore the harmonic level can vary is slow in comparison.

Also, as the only significant source of energy storage in the SC is the ESS, $P_c > 0$ would indicate an export of power from the SC to the external system. It will cause a decrease in the voltage $\mathbf{V}_{dc}$ across the ESS. Conversely $\mathbf{V}_{dc}$ will begin to rise if the SC starts to import **P**c from the external system. Variations of $\mathbf{V}_{dc}$ will affect the compensation capability of the SC and excessive voltage rise will damage the ESS. Hence $\mathbf{V}_{dc}$, has to be controlled within acceptable range, that is, Pc has to be regulated. Fig. 3(b) shows the Phasor diagram of hth harmonic order compensation by the SC. For perfect harmonic voltage cancellation, the ideal voltage injected by the SC is –V'sh but due to the SC bandwidth limitation described earlier, the actual voltage injected is $-\vec{\mathbf{V}}'_{sh}$ Although the phase difference between $\vec{\mathbf{V}}_{sh}$ and $-\vec{\mathbf{V}}'_{sh}$ would depend on the SC controller design, this phase difference is expected to be small in practice if the cancellation is to be reasonably effective. Since the sensitive load is assumed to be resistive-capacitive, the **h**th harmonic voltage component across the load $\vec{\mathbf{V}}_{Lh}$ lags the harmonic current $\mathbf{I}_{Lh}$. The phase angle θ_h between $-\vec{\mathbf{V}}'$sh and $\vec{\mathbf{I}}$ Lh between and is therefore larger than 90, as shown. Thus the harmonic power $P_{Ch} = \sum_{h=2}^{\infty} \mathrm{Re}\{-\vec{V}'_{Sh}\vec{I}^{*}_{Lh}\} > 0,$ that is, the SC will import real power $\mathbf{P}_{ch}$ from the external system. The extent of the power import will depend on the injection voltage, which, in turn, depends on the main drive load operating conditions. This aspect will be examined in greater details next.

2.3 Harmonic Power Flow

In Fig. 4, the main load is shown as a dc drive system. The dc motor, represented by the equivalent RL circuit, is assumed to be fed by a six-pulse controlled converter. The firing angle of the converter determines the average value $\mathbf{V}_d$ of the output voltage. The converter output current can be controlled via a PI regulator which changes δ_1. In this way, the effect of a load change can be readily studied by altering the reference current $\mathbf{I}_{ref}$. The main converter load is the dominant harmonic source in the power system due to its much larger capacity, compared to the SC and sensitive load. The SC is assumed to be "ideal" in that whatever harmonics generated by the VSI are effectively dealt with by its LC filter. The SC is a harmonic "sink." In this way, $\mathbf{P}_{Dh}$ the harmonic power produced by the nonlinear main drive load is dissipated in the upstream source impedance and is Absorbed by the sensitive load. The harmonic power flow to the upstream source $\mathbf{P}_{sh}$ and into the sensitive load $\mathbf{P}_{Lh}$ are as shown in Fig. 4.

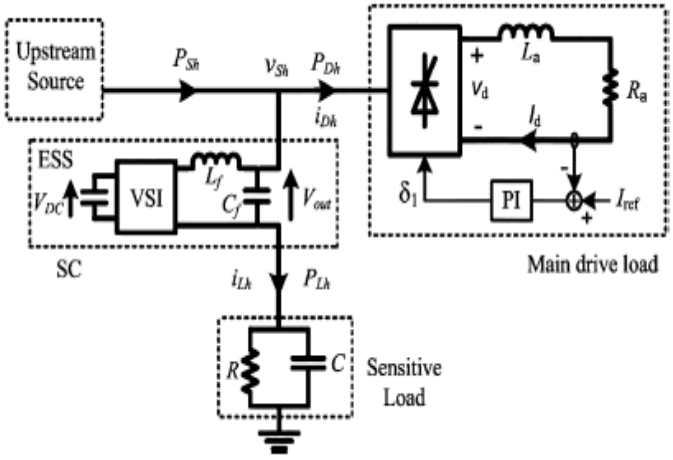


Fig. 4: Harmonic power flow in the isolated system: hth harmonic component.

To assess the value of $\mathbf{P}_{Dh}$, the harmonic contents of Vs(t) and **i**D(t) have to be known. In order to do so, the following assumptions are made: the upstream source consists of balanced sinusoidal EMF of constant voltage with equal inductances; its phase "a" terminal voltage is of the form $V_{s1}(t) = V_m \sin\omega_0 t$ and $\mathbf{I}_d$ is assumed to be ripple free. The firing angle δ_1 changes as load condition varies and in general, δ_1 and δ_2 the overlap angle of the converter determine the exact waveform of Vs(t). Harmonic components of Vs(t) and **i**D(t) and could be obtained through Fourier analysis and can be evaluated. Furthermore, once Vs(t) has been determined, P_{sh} can also be determined as the source impedance Z_s is assumed known. The balance of the harmonic power is diverted to the SC branch. Part of this $\mathbf{P}_{Lh}$ harmonic power will be absorbed by the sensitive load. Once P_{Dh},$\mathbf{P}_{Lh}$, and $\mathbf{P}_{sh}$ have been obtained, the harmonic power imported by the SC, $\mathbf{P}_{ch}$ could be evaluated. Numerical cases are used to illustrate how the harmonic power flow in the network can be assessed.

Case1: Suppose the ratio between the VA capacity of the main drive load and that of the sensitive load is k. The upstream source fault level is "m" times that of the main drive load capacity. The X/R ratio of Zs at the fundamental frequency is q , that is, $X_{S1}/R_S = q.$.

Assume the drive-load converter operates at δ_1 = 10° and an overlap angle δ_2 = 20° the resulting waveforms of **V**s(t) and **i**D(t) can be derived. Fourier analysis of Vs(t) and **i**D(t) yields the following characteristic harmonic components

$$v_{Sh}(t) = \hat{V}_m[0.28\sin(5\omega_o t + 70^\circ) + 0.16\sin(7\omega_o t + 75^\circ) + 0.1\sin(11\omega_o t + 56^\circ) + \cdots] \quad (12)$$

$$i_{Dh}(t) = 3.46 \times \frac{I_d}{\pi}\left[\frac{1}{5}\sin(5\omega_o t - 50^\circ) + \frac{1}{7}\sin(7\omega_o t + 110^\circ)\frac{1}{11}\sin(11\omega_o t - 110^\circ) + \cdots\right]. \quad (13)$$

From (12) and (13), the harmonic power $\mathbf{P}_{Dh}$ (up to the 11th harmonic) generated by the main drive load can be obtained:

$$P_{Dh} = \frac{3}{2}\sum_{h=5}^{11}\hat{V}_{hm}\hat{I}_{hm}\cos(\varphi_k - \sigma_k) = -0.032\hat{V}_m I_d.$$

… (14)

The average dc voltage can be calculated:

$$V_d = 1.65\hat{V}_m(\cos\delta_1 + \cos(\delta_1 + \delta_2))/2 = 1.53\hat{V}_m \quad (15)$$

And, therefore, the power of the fundamental frequency component of the main drive load is

$$P_{D1} = V_d I_d = 1.53\hat{V}_m I_d. \quad (16)$$

The converter is assumed lossless. Using $\mathbf{P}_{D1}$ and V_m as base values, the harmonic power exported by the main load is

$$P_{Dh} = -0.02 \text{ p.u.} \quad (17)$$

As the system short-circuit ratio is m and Xs1/Rs = q can be calculated. Apply

$P_{Sh} = \sum_{h=5}^{11} Re\{\vec{V}_{Sh}\vec{I}^*_{Sh}$ it can be readily shown that

$$P_{Sh} = -\frac{0.0014m}{q^2} \text{ p.u.} \quad (18)$$

Next, suppose the THD of the voltage at the terminals of the sensitive load is to be limited to (say) 3%. Thus, **P**Lh can be obtained

$$P_{Lh} = \frac{(\text{THD}_V)^2}{k} \approx \frac{0.001}{k} \text{ p.u.} \quad (19)$$

Hence, the harmonic power imported by the SC is estimated to be:

$$P_{Ch} = P_{Sh} - P_{Dh} - P_{Lh} = \left(0.02 - \frac{0.0014m}{q^2} - \frac{0.001}{k}\right) \text{ p.u.} \quad (20)$$

As an illustration, for typical values of m = 10, q =5 and k = 10. the last expression shows that Pch ≈ 0.019 p.u . Since it is assumed that the sensitive load capacity is 1/10 that of the main drive load, therefore $\mathbf{P}_{ch}$ corresponds to some **19%** of the sensitive load capacity.

Case 2: If the converter operates at $\delta_1 = 30°$ and $\delta_2 = 25°$ instead, Fourier analysis of and yields

$$v_{Sh}(t) = \hat{V}_m[0.18\sin(5\omega_o t - 140^\circ) + 0.24\sin(7\omega_o t - 129^\circ) + 0.08\sin(11\omega_o t - 148^\circ) + \cdots] \quad (21)$$

$$i_{Dh}(t) = 3.46 \times \frac{I_d}{\pi}\left[\frac{1}{5}\sin(5\omega_o t + 30^\circ) + \frac{1}{7}\sin(7\omega_o t - 30^\circ) + \frac{1}{11}\sin(11\omega_o t + 30^\circ) + \cdots\right]. \quad (22)$$

Then, following the same procedure as shown earlier, one can show that:

$$P_{Dh} = -0.08\hat{V}_m I_d, V_d = 1.19\hat{V}_m,$$
$$P_{D1} = V_d I_d = 1.19\hat{V}_m I_d,$$
$$P_{Dh} = -0.067 \text{ p.u.}, P_{Sh} = -\frac{0.0006m}{q^2} \text{ p.u.}$$
$$P_{Lh} \approx \frac{0.001}{k} \text{ p.u.}$$

The harmonic power imported by the SC is

$$P_{Ch} = P_{Sh} - P_{Dh} - P_{Lh} = \left(0.067 - \frac{0.0006m}{q^2} - \frac{0.001}{k}\right) \text{ p.u.} \quad (23)$$

In this case, P_{ch} is seen to be equivalent to some 67% of the sensitive load capacity, if the same numerical values of m, q and k used earlier were again assumed. This is a substantial amount of absorbed power, in so far as the sensitive load is concerned. The above examples serve to illustrate that the operating states of the converter will affect the harmonic power exported by the main load which, in turn, determines the amount of the harmonic power absorbed by the SC. The dominant factor governing P_{ch} appears to be P_{Dh} that is, a significant part of P_{Dh} will be absorbed by the SC.

3. VOLTAGE RESTORATION IN ISOLATED POWER SYSTEM

Having considered harmonic power flow in the isolated power system, voltage restoration will be examined next. As stated earlier, voltage control of the ESS is necessary to ensure the proper operation of the SC and to protect the device. Thus it is desirable to regulate the power transfer between the SC and the external system so that V_{dc} across the ESS of the SC can be maintained. Once this is achieved, the SC will be able to exercise network voltage control; The SC will assume this role of voltage control until such time when the excitation system of the upstream generator becomes effective in forcing the generator to share the voltage regulation duty. However, if the excitation system is a slow-acting electromechanical type, the sensitive load would have to rely very much on the SC to achieve a constant $\mathbf{V}_L$. It is therefore necessary to examine the extent by which the SC can exercise such control. Furthermore, in terms of voltage quality, it is the fundamental component $\mathbf{V}_L$ of which is of the greatest importance. Hence in what follows, the focus is on maintaining the magnitude of this voltage component $\vec{V}_{L1}$, denoted as in Fig. 5.

The condition of zero power transfer between the SC and the external system is examined first. From (11), this means that $P_C = P_{C1} + P_{Ch} = 0$, that is, when

$$P_{C1} = -P_{Ch}. \qquad (24)$$

It is concluded that the SC absorbs harmonic power from the external system, that is, $\mathbf{P}_{ch} > 0$. Thus, from (24), at zero power transfer, the SC should export power of the fundamental frequency component equal to an amount $\mathbf{P}_{ch}$ in order to balance the imported harmonic power. Next, define an equivalent fundamental frequency component voltage $\mathbf{V}_p$ of the SC injected voltage $\mathbf{V}_{out}$ such that:

$$V_P I_{L1} = P_{Ch}. \qquad (25)$$

The last expression means that when the projection of the fundamental frequency component of $\mathbf{V}_{out}$ (shown as in Fig. 5) onto is $\vec{\mathbf{I}}_{L1}$ is V_p, the condition for zero power transfer is reached.

3.1 Voltage Swell

When the drive load varies and causes a voltage swell, $\mathbf{V}_{s1} > \mathbf{V}_{L1}$, as shown in Fig. 5(a), where $\mathbf{I'}_{L1}$ is shown as the reference Phasor. Since $\mathbf{V}_{L1}$ denotes the desired voltage magnitude at the sensitive load terminals, the aim is to maintain it constant through the action of the SC. Assume the sensitive load is of constant power factor at the fundamental frequency. Therefore from (11), $\theta = \varphi_{11} + \alpha$, that is, the phase angle between $\vec{\mathbf{I}}_{L1}$ and $\mathbf{V}_{L1}$ is constant at θ . α is the phase shift described in Section II. From (7), the SC injected voltage is $\vec{V}_1 = \vec{V}_{L1} - \vec{V}_{S1}$ and since $\mathbf{P}_{c1} = \mathrm{Re}\{\vec{\boldsymbol{V}}1\vec{\boldsymbol{I}}^{*}_{L1}\}$, $\mathbf{P}_{c1}$ can

$$P_{C1} = \frac{1}{2}[V_{L1}\cos\theta - V_{S1}\cos(\theta - \alpha)] \cdot I_{L1}. \qquad (26)$$

The situation depicting $\vec{V}_{L1}$ and $\vec{V}_{s1}$ by the solid lines in Fig. 5(a) shows that **P**c1 is negative. This corresponds to the situation when the SC imports P_{c1} from the external system. By continuously adjusting and shifting $\vec{V}_{s1}$ in the clockwise direction, P_{c1} will become less and less negative and it eventually will become positive, that is, the SC will then export Pc1 to the external system. The condition shown by the dotted lines in Fig. 5(a) is when the projection of $\vec{\boldsymbol{V}}_1$ onto $\vec{\boldsymbol{I}}_{L1}$ is equal to the value of $\mathbf{V}_p$ given by (25) precisely. Hence, at this point, the SC output power contributed by the fundamental frequency component voltage and current is $V_P I_{L1} = P_{C1} > 0.$. Again from (25), $P_{C1} + P_{Ch} = 0$ and thus zero power transfer condition between the SC and the external system is reached. Mathematically, this can be expressed by the condition when

$$V_{L1}\cos\theta - V_{S1}\cos(\theta - \alpha) = V_P. \qquad (27)$$

Hence, at this zero power transfer condition, the phase angle between $\vec{\boldsymbol{V}}_{s1}$ and $\vec{\boldsymbol{V}}_{L1}$ is α_0 where

$$\alpha_0 = \theta - \arccos\left(\frac{\cos\theta - \beta}{\gamma}\right) \qquad (28)$$

$$\gamma = \frac{V_{S1}}{V_{L1}}, \quad \beta = \frac{V_P}{V_{L1}}. \qquad (29)$$

For a voltage swell, α_0 is negative, that is, $\vec{\boldsymbol{V}}_{s1}$ lags $\vec{V}_{L1}$ at zero power transfer. At this instance, the phase angle of is $\mathbf{V}_{s1}$ is $arccos\,[(\cos\theta - \beta)/\gamma]$. Furthermore, one concludes that the SC will import power, $\mathbf{P}_c = \mathbf{P}_{c1} + \mathbf{P}_{ch} < 0$ when $\alpha < \alpha_0$ that is, $\vec{\boldsymbol{V}}_{s1}$ is shifted in the counterclockwise direction from the condition $\alpha = \alpha_0$. Conversely, if α were adjusted in the clockwise direction, and as the projected component $\vec{\boldsymbol{V}}_1$ onto $\vec{\boldsymbol{I}}_{L1}$ is larger than,

$\mathbf{V}_p$ then $\mathbf{P}_C = \mathbf{P}_{c1}+\mathbf{P}_{ch} > 0$. The SC would then export power to the external system.

The above analysis suggests a method to regulate the ESS voltage $\mathbf{V}_{dc}$. If $\mathbf{V}_{dc}$ decreases below a set value, it means that the SC is exporting total power Pc to the external system. One can then reverse the fall in $\mathbf{V}_{dc}$ by adjusting the VSI firing angle to effect a counter-clockwise phase shift $\vec{\boldsymbol{V}}_{s1}$ in such that $\alpha < \alpha_0$, in order to force a net import $\mathbf{P}_c$ of and vice-verse. In this way, $\mathbf{V}_{dc}$ can be regulated through the control of $\boldsymbol{\alpha}$. Since the power factor angle θ , the factors β and γ (as defined by (29)) can be readily determined online, the calculation α_0 for can be accomplished as part of the SC real-time control system. The phase-shift control strategy to regulate P_c can be realized. It is interesting to note that from (25), if $\mathbf{P}_{ch}$ increases due to drive load changes, V_p and α_0 will also increase. This means that $\vec{\boldsymbol{V}}_1$ also increases. Hence, the SC voltage rating has to be adequate in order to cater for this injection method.

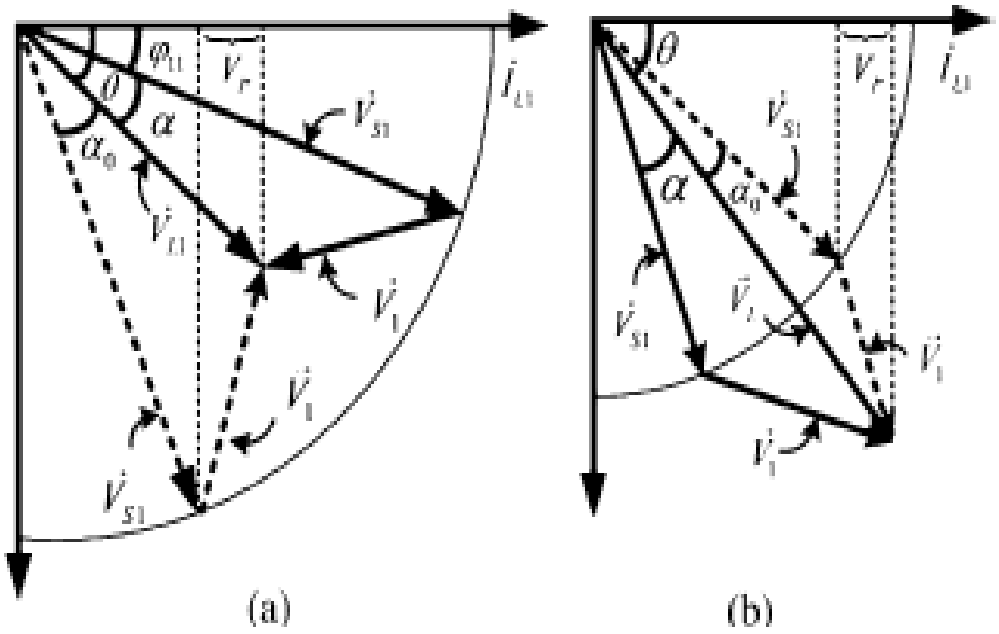


Fig.5: Phasor diagram showing voltage restoration during (a) voltage swell and (b) voltage sag: fundamental frequency component.

3.2 Voltage Sag

The above analysis can be extended to deal with the event of voltage sag, that is, $V_{s1} < V_{L1}$. Fig. 5(b) shows a general Phasor diagram during voltage sag. By similar reasoning as shown for voltage swell $P_c < 0$, when α_0 is positive.

$$\alpha > \alpha_0 = \theta - \arccos\left(\frac{\cos\theta - \beta}{\gamma}\right) \qquad (30)$$

Phase shifting of $\vec{\boldsymbol{V}}_{s1}$ can lead to zero power transfer when $\boldsymbol{\alpha} = \boldsymbol{\alpha}_0$. This is shown by $\vec{\boldsymbol{V}}_{s1}$ and $\vec{\boldsymbol{V}}_1$ in dotted lines in the figure. From this condition of zero power transfer, if one were to adjust to $\vec{\boldsymbol{V}}_{s1}$shift it in the counter-clockwise direction $\mathbf{P}_c < 0$, when $\vec{\boldsymbol{V}}_{s1}$ leads $\vec{\boldsymbol{V}}_{L1}$ by an angle α where $\boldsymbol{\alpha} > \boldsymbol{\alpha}_0$.The SC then imports power from the external system. Conversely, adjusting $\vec{\mathbf{V}}_{s1}$ in the clockwise direction can lead to $\boldsymbol{\alpha} < \boldsymbol{\alpha}_0$. When this occurs, $\mathbf{P}_c < 0$, the SC will export real power to the external system. An example of such a condition is shown by $\vec{\boldsymbol{V}}_{s1}$ and $\vec{\boldsymbol{V}}_1$ the solid lines shown in Fig. 5(b). Hence if it is noted that $\mathbf{V}_{dc}$ is above a set value, it will then be necessary to introduce a phase shift $\boldsymbol{\alpha}$ in $\vec{\boldsymbol{V}}_{s1}$ in such that. $\boldsymbol{\alpha} < \boldsymbol{\alpha}_0$. The SC then exports real power to the external system. The ESS voltage should decrease. Conversely, if $\mathbf{V}_{dc}$ is below the set value, $\vec{\mathbf{V}}_{s1}$ phase should be adjusted to meet the condition $\alpha > \alpha_0$.

Fig. 6(a) shows the condition in which the severity of the sag is such that. $\mathbf{V}s1/\mathbf{V}L1 = \boldsymbol{\gamma} < \cos\theta$ It can be seen that by $\vec{\mathbf{V}}_{s1}$ shifting until it aligns with $\mathbf{I}_{L1}$, $\mathbf{P}_{c1}$. is exported from the ESS to the external system at the minimum value. This is the condition indicated by $\hat{V}_1$ assuming the position of the dotted line in the figure. The minimum exported power is

$$\mathbf{P}_{c1min} = \mathbf{V}_{L1}.\,\mathbf{I}_{L1}(\cos\theta-\gamma). \qquad (31)$$

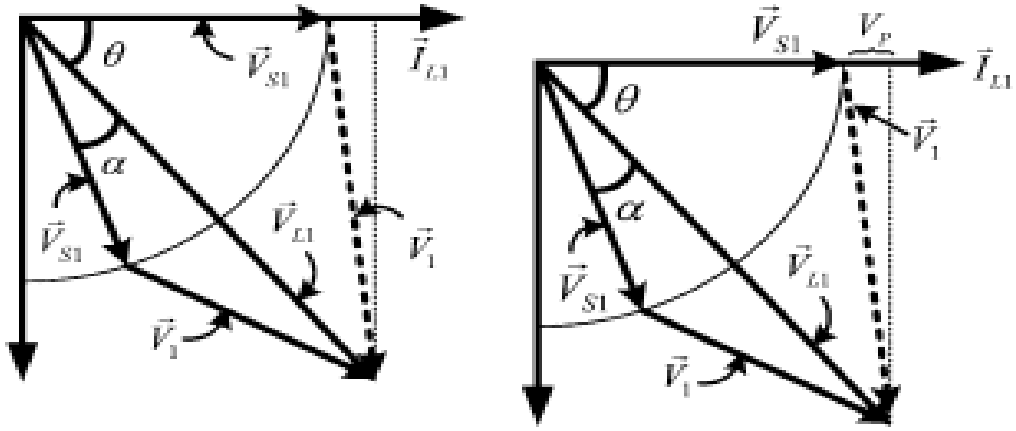


Fig.6. Phasor diagram of voltage sag condition when $V_{s1}/V_{L1} = \gamma < cos\theta$: (a) without harmonic power taken into consideration and (b) with harmonic power taken into consideration.In the event if $\mathbf{V}_{dc}$ is already lower than its desirable set value, one would need to adjust α in such a way that $\mathbf{P}_{c1}$ can be absorbed from the external system. From the Phasor diagram, however, it shows that it is impossible to affect such a condition for power absorption.At best, $\vec{V}_{s1}$ with adjusted to be in-phase with, the SC exports $\mathbf{P}_{c1}$ at the minimum value given by (31). It can only minimize the rate of the decrease of V_{dc}. With the harmonic power flow included in the compensation process, the situation improves somewhat. Fig. 6(b) shows the most severe sag that can be compensated for when $\hat{V}_{s1}$ is shifted to be in phase with

$\vec{I}_{L1}$, and the harmonic power $\mathbf{P}_{ch}$ absorbed by the SC is given by (25), that is, , $\mathbf{P}_{ch} = -\mathbf{V}_p\mathbf{I}_{L1}$ with being equal to that shown in the figure. In this way, zero power exchange between the SC and the external system has been achieved. From Fig. 6(b), it is seen that

$$V_{S1} + V_P = V_{L1}\cos\theta. \qquad (32)$$

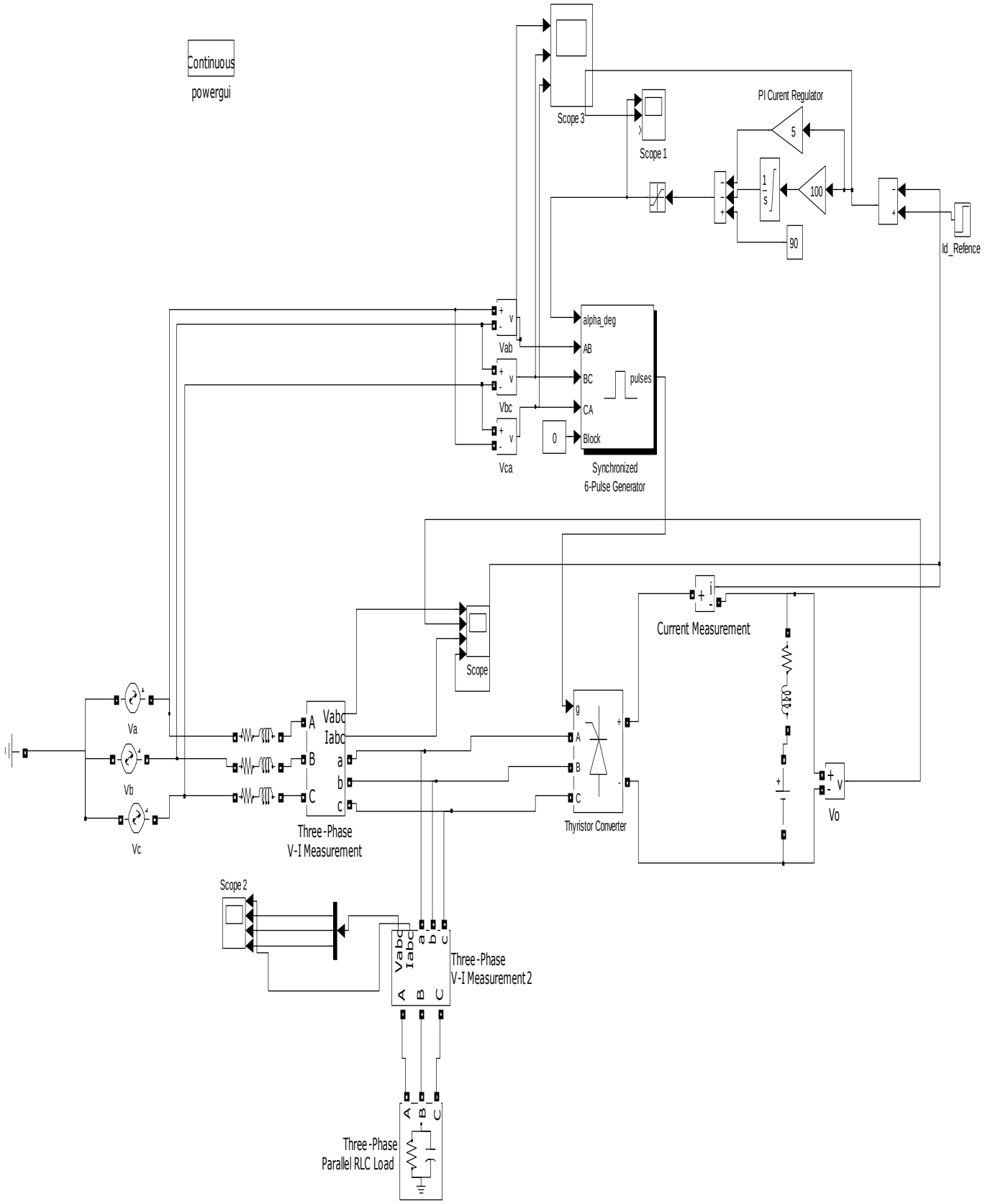
Hence, the most severe voltage sag that the SC can compensate for while maintaining zero power transfer is

$$\gamma_{min} = \cos\theta - \beta \qquad (33)$$

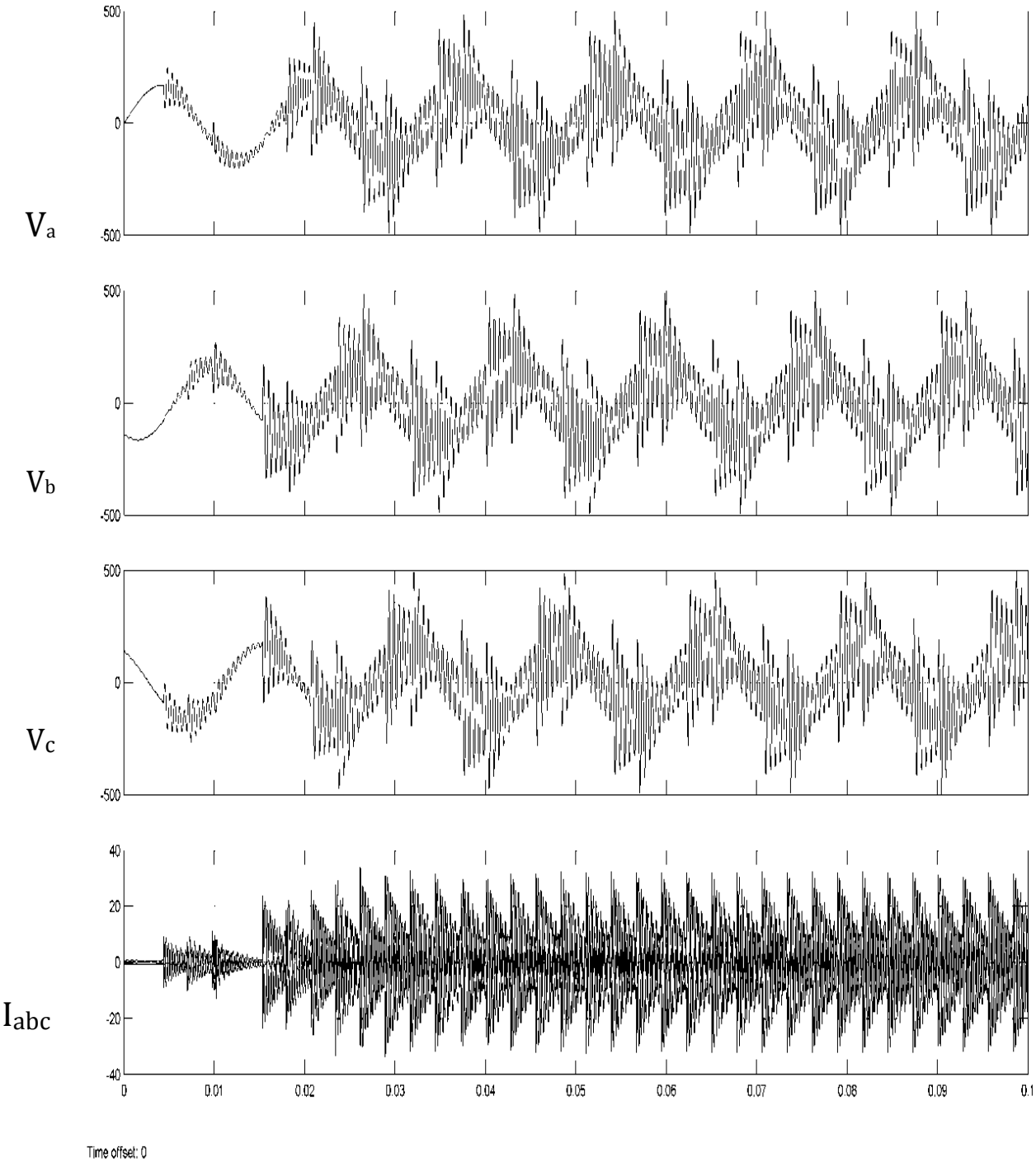
Where, as defined by (29), $\gamma = V_{s1}/\mathbf{V}_{L1}$, $\beta = \mathbf{V}_p/\mathbf{V}_{L1}$ Hence, by adjusting and taking advantage of the presence of the harmonic power $\mathbf{P}_{ch}$, the proposed compensation strategy compares Favorably with that shown in Fig. 6(a) where the most severe sag that can be

Compensated for is cosθ, if $\mathbf{V}_{dc}$ is to be maintained constant. The proposed method improves the ride through capability of the sensitive load by a margin β, through the SC absorbing the harmonic power generated by the main load and converting it into real power for supporting the sensitive load voltage. From (33), clearly the most onerous ride through condition is when the sensitive load power factor is unity. Also, the following observations can also be arrived at. Since $\beta = \mathbf{V}_p/\mathbf{V}_{L1}$, β decreases with $\mathbf{V}_p$. However, from (25), it is seen that V_p decreases with an increase in I_{L1} for a given P_{ch}. Hence, the margin β would be at the minimum when **I**L1 is at its maximum value (i.e., when the sensitive load is at full load). $\mathbf{P}_{ch}$ depends most significantly on $\mathbf{P}_{Dh}$ which in terms bears a complex relationship to the operating state of the motor drive. While it is difficult to generalize this relationship, it is clear that when the motor load is at full load, full-conduction in the rectifier occurs and harmonic distortions are expected to be at the minimum. Hence $\mathbf{P}_{Dh}$, and correspondingly $\mathbf{P}_{ch}$, will be at the minimum. Again from (25), $\mathbf{V}_P$ and therefore, β will be at the minimum. Based on the above observation, it can therefore be concluded that One most sensitive load ride through condition would be when the load is at full load, unity power factor, while $\mathbf{P}_{Dh}$ is at the minimum or when the motor load is operating at rated power. Also from (33), one notices that the most severe voltage-sag that the SC can provide load ride through is when $\gamma = \gamma_{min}$. For small β, γ_{min} is approximately equal to the load power factor. From Fig. 6(b), the maximum injection voltage is approximately equal to $\mathbf{V}_{L1}$ sinθ. Hence, the SC must be rated to be at least sinθ times that of the sensitive load. Although not shown in the above analysis, similar conclusions can also be reached if the power factor of the sensitive load is lagging.

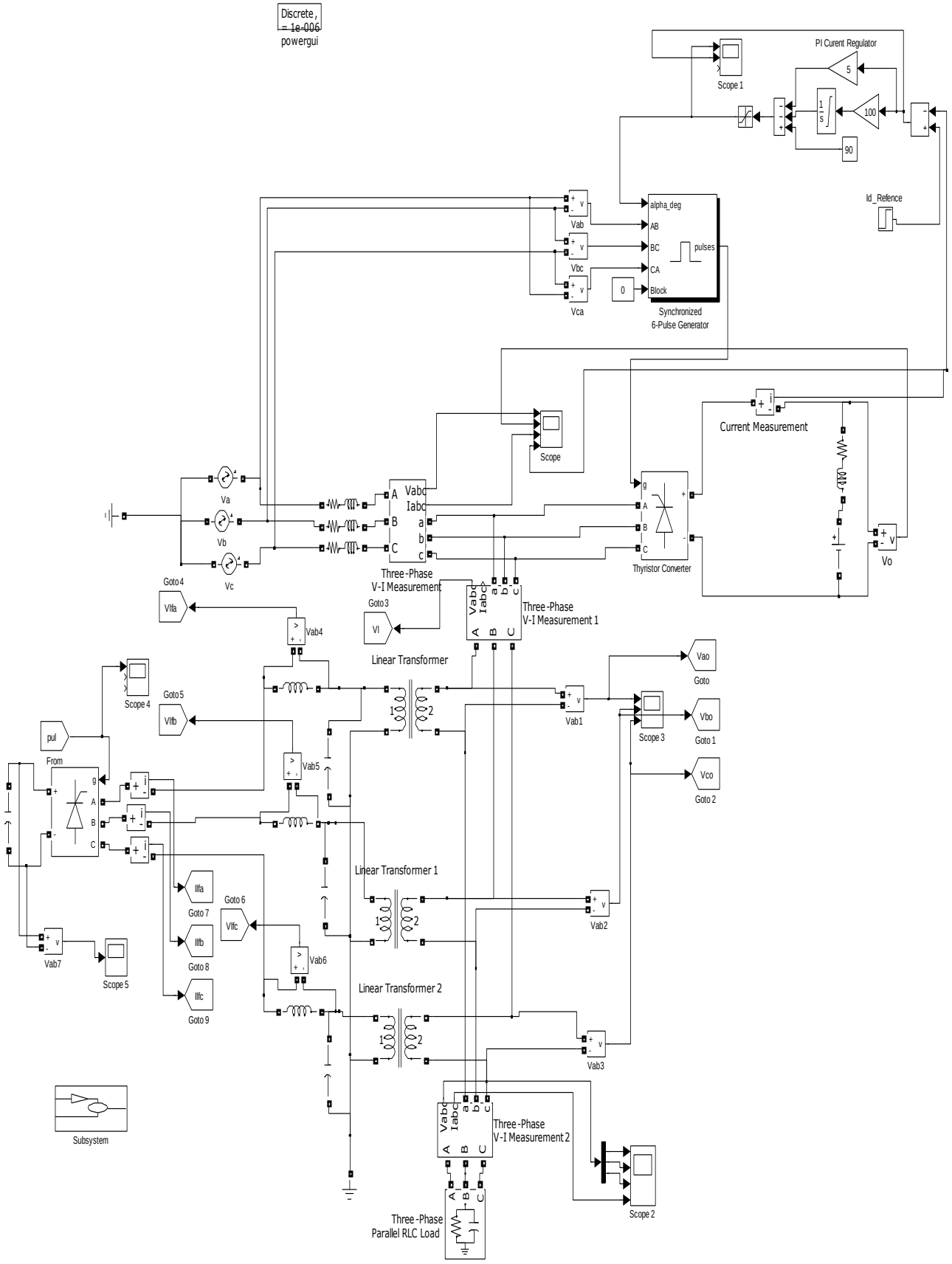
4. SIMULINK DIAGRAM OF ISOLATED POWER SYSTEM WITHOUT SERIES COMPENSATOR



4.1 Output Voltage & current waveforms without series compensator

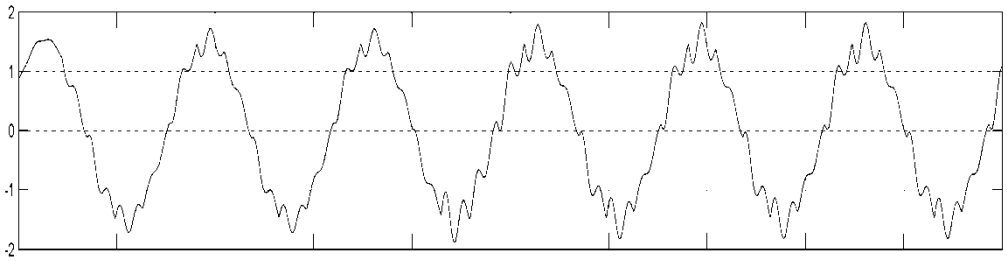


4.2 Simulink diagram of isolated power system with series compensator

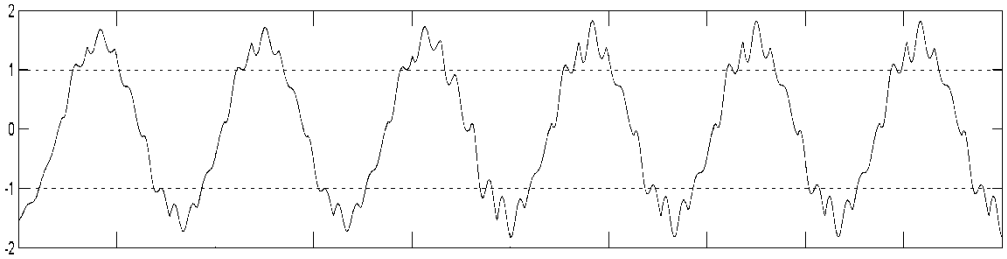


4.3 Output voltage & current wave forms with series compensator

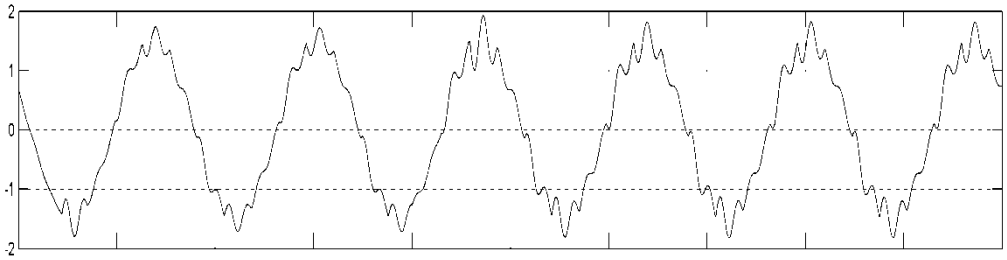
V_a .



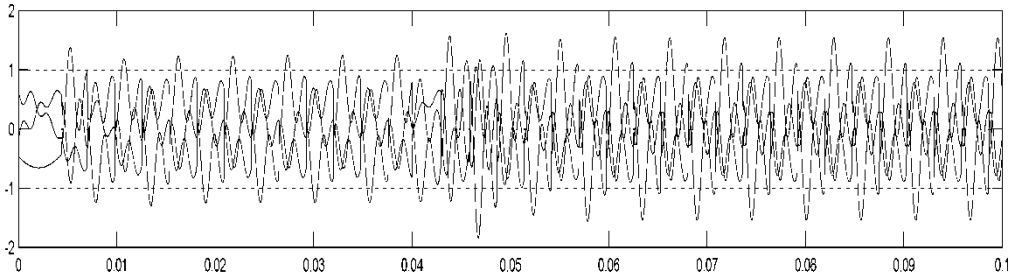
V_b



V_c



I_{abc}



5. CONCLUSIONS

Voltage quality improvement in an isolated power system through series compensation has been investigated. It is observed that the power system contains significant proportion of fluctuating nonlinear load and high level of harmonic distortions. A method to control the injection voltage of the series compensators(SC)so that it can mitigate the effects of the harmonics has been proposed. The SC is also designed to maintain the fundamental frequency component of the terminal voltage of protected sensitive load. In the process of harmonic voltage compensation, it is shown that power exchange exists between the SC and the external network. Based on the analysis of the harmonic real power flow in the power system, it is seen that the SC would import harmonic real power from the external system. A new SC control strategy is then proposed which involves the phase adjustment of the fundamental frequency component of the sensitive load terminal voltage. Through the analysis of the power exchange, it is shown that the load ride through capability during

voltage sag can be improved with the support of the harmonic real power absorbed by the SC. The capacity of the SC required is modest and, therefore, makes it a viable device for such an application. Simulations have confirmed the effectiveness of the proposed method, as it is applied on the SC to achieve improved quality of supply in the power system.

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NOMENCLATURE

$\mathbf{V}s$, $\mathbf{V}_{s1}$, $\mathbf{V}_{sh}$ Upstream source voltage, its fundamental and harmonic components, respectively.

$\mathbf{V}_L$, $\mathbf{V}_{L1}$ Terminal voltage of the sensitive load and its fundamental component.

$\mathbf{V}_{out}$ Injected voltage of the SC.

$\mathbf{V}_{s1}$ Phasor of the fundamental component of the source voltage.

$\vec{\mathbf{V}}_1$ Phasor of the fundamental component of the SC injected voltage.

$\overrightarrow{\mathbf{V}}_{L1}$ Phasor vector of the fundamental.

$\mathbf{V}_{s1}$ RMS value of the fundamental component of the source voltage.

$\mathbf{V}_{L1}$ RMS value of the fundamental component of the sensitive load voltage.

$\mathbf{V}_p$ Equivalent fundamental component of **V**out Where $V_p\mathbf{I}_{L1} = \mathbf{P}_{ch}$.

$\mathbf{I}_L$ Sensitive load current.

$\mathbf{P}_s$, $\mathbf{P}_{s1}$, $\mathbf{P}_{sh}$ Power flow on source side, its fundamental and harmonic components, respectively.

$\mathbf{P}_D$, $\mathbf{P}_{D1}$, $\mathbf{P}_{Dh}$ Power flow of main loads, its fundamental and harmonic components, respectively.

$\mathbf{P}_c$, $\mathbf{P}_{c1}$, $\mathbf{P}_{ch}$ Power flow of the SC, its fundamental and harmonic components, respectively.

δ_1 Delay angle of converter.

δ_2 Overlap angle of converter.

$\cos\theta$ Sensitive-load power factor at the fundamental frequency.

α_0 Phase angle between $\vec{\mathbf{V}}_{s1}$ and $\vec{\mathbf{V}}_{L1}$ at the condition $\mathbf{P}_c = 0$

γ Ratio of $\mathbf{V}s1/\mathbf{V}$ L1.

β Ratio of $\mathbf{V}_p/\mathbf{V}_{L1}$.

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