iJET EXPLORE International Journal of Engineering & Technology
CENTRE OF PROFESSIONAL RESEARCH PUBLICATIONS
ISSN 2049-3444

International Journal of Engineering and Technology Volume 2 No. 4, April, 2012

Certain Investigations on Static Power Dissipation in various Nano-Scale CMOS D Flip-Flop Structures

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ABSTRACT

In this paper the impact of existing leakage current reduction techniques on Various D Flip Flop Circuits are analyzed and summarized. As Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices are scaled down to nanometer ranges, Complementary MOS (CMOS) circuit's total Power consumption has a new definition. Due to integration of millions of components and shrinking process technology, nowadays leakage power tends to play a major role in total power consumption. This fact has motivated a lot of researchers and technologists to choose leakage current minimization as their future work. This paper explores various D flip-flop topologies meant for different constraints such as speed, area and power. Proper selection of flip-flops is necessary in order to satisfy low power and high performance circuit. In this paper, different flip flop circuits are designed using 16nm Metal gate, High-K dielectric, Silicon on Insulator (SOI) Low Power Predictive Technology Model (PTM) file developed based on Berkeley Short Channel Insulated Gate MOSFET (BSIM) model equations. As the estimation of leakage at circuit level is of prime importance for VLSI engineers, this paper aims at implementation of both active and standby mode leakage power reduction techniques. Of the available techniques, six techniques are considered for the purpose of analysis namely Multi Threshold CMOS (MTCMOS), Super Cut-off CMOS (SCCMOS), Forced Transistor Stacking (FTS) and Sleepy Stack (SS)**.** From the results, it is observed that MTCMOS and SCCMOS techniques produces lower power dissipation than the other techniques due to the ability of power gating. As there were no previous works reported related to comparison of power analysis of 16nm devices with the above leakage reduction techniques, in this paper a qualitative comparison is done with the help of TannerSPICE Circuit Simulation Tool. After a detailed analysis of the existing techniques, this paper concludes that same leakage reduction technique produce different power optimization levels for different architectures and employing a suitable technique for a particular architecture will be an effective way of reducing the leakage current and thereby static power.

Keywords: *CMOS, MOSFET, D Flip Flop, Leakage current, Forced Transistor Stack, Multiple Threshold, Super-Cutoff*

1. INTRODUCTION

In early 1970's, the main design focuses were providing for high-speed operation and a design with minimum area, design tools were all concentrated in achieving these two goals. Due to the advent of portable systems, low-power design is becoming the foremost requirement of all high-performance applications, as power is the most important single design constraint. In the present scenario, power dissipation has become a major challenge and its management is a critical technology in the electronics industry. In the submicron technologies, the static power dissipation caused by leakage currents and sub threshold currents contribute a small percentage to the total power consumption, while the dynamic power dissipation, resulting from charging and discharging of parasitic capacitive loads of interconnects and devices dominates the overall power consumption.

But as technologies scales down to the nanometer regime (Ultra Deep Sub-Micron (UDSM)), the static power dissipation becomes more dominant than the dynamic power consumption. And despite the aggressive downscaling of device dimensions and reduction of supply voltages, which reduce the power consumption of the individual transistors, the exponential increase of operating frequencies results in a steady increase of the total power consumption. With technology downscaling, interconnect resistance and capacitance increase the propagation delay. Leakage power optimization will be a key design objective in future CMOS circuits. Moreover, power optimization is beneficial as it lowers packaging and cooling costs and hence improves reliability of the

circuit. As predicted by International Technology Roadmap for Semiconductors (ITRS) [1], power will continue to be a limiting factor in future technologies. Two major factors for the increase in power dissipation are the speed and the number of gates on the silicon[2].

The two main effects that contribute to the total power dissipation on a chip are the active and static power dissipation. The expression to compute the total power is as follows

$$P_{total} = P_{dynamic} + P_{sc} + P_{static} \quad (1)$$

Dynamic dissipation power occurs when a transistor switches state and is due to capacitive charging and discharging associated with the output wiring. A small proportion of dynamic power arises from the short-circuit current that flows momentarily while the complementary devices (push/pull) in a circuit are simultaneously conducting during a change in the output state. This dynamic power is considerable during normal mode of operation, especially at high operating frequencies. The dynamic power consumption (P_{dyn}) is given by

$$P_{dyn} = kCV_{dd}^2 f_{sw} \quad (2)$$

Where k is the technology factor, C is the capacitance of switching nodes, V_{dd} is the supply voltage and f_{sw} is the effective switching frequency. During the transition of signals from $0 \rightarrow 1$ or from $1 \rightarrow 0$, both nmos and pmos network of CMOS circuits will be on for a while which leads to short-circuit power dissipation (P_{sc}) and given by

$$P_{sc} = I_{sc}.V_{dd}.t_s.f_{sw} \quad (3)$$

Where I_{sc} is the short circuit current, t_s is the switching delay. Both sources of power dissipation (P_{dyn} and P_{sc}) in CMOS circuits are related to transitions at gate outputs and are therefore collectively referred to as active dissipation. In contrast, the third source of power dissipation (P_{static}) is due to leakage current, which flows when the inputs and outputs are changing their state and is called static dissipation (P_{static}). In standard CMOS circuits, only static dissipation is due to leakage current, usually small in magnitude and will be computed by

$$P_{leak} = I_{leak}.V_{dd} \quad (4)$$

But as the supply voltage is being scaled down to reduce dynamic power, lower threshold transistors have to be used to maintain performance, yet the lower the threshold voltage, greater the standby leakage current. Due to the substantial increase in leakage current, the static power consumption is expected to exceed switching portion of power consumption unless effective measures are taken to reduce leakage power. If we look in to the major challenges faced by sub 32nm CMOS era, leakage power plays a vital role in deciding the overall power consumption [3]-[4]. In many recent designs, the leakage power dissipation is on par with the dynamic power. It is foreseen that 50% or even higher percentage of the total power consumption will be due to the leakage current in future CMOS devices and this percentage will be increasing with scaling down of device dimensions unless effective leakage control techniques are investigated and used while designing the nanoscale circuits to bring leakage current under control [5].

This paper is organized as follows: Section 2 presents an overview of major leakage current mechanisms of Nanoscale CMOS circuits. A brief review of leakage reduction technique is given in section 3. Section 4 describes about the experimental setup made for performance analysis. Results of average power, leakage current, leakage power, delay, percentage of average and leakage power reduction are discussed in section 5. Finally, conclusions are presented in section 6.

2. OVERVIEW OF LEAKAGE CURRENT MECHANISMS

There are six short-channel leakage mechanisms as illustrated in Fig1.

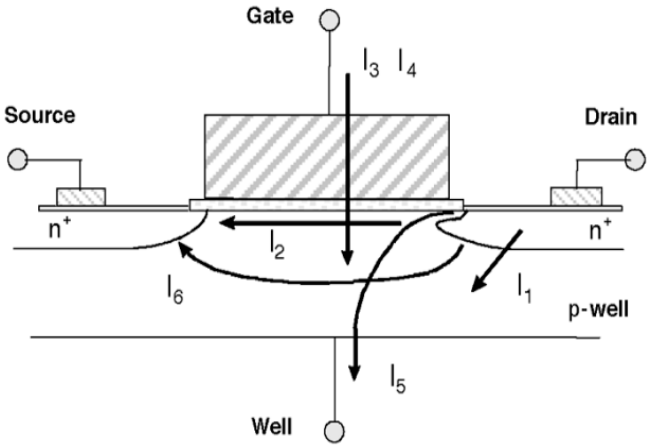

Fig1: leakage current mechanisms in deep-sub micrometer transistors[3].

Drain and source to well junctions form PN junction and are typically reverse biased during the operation which causes PN junction leakage current flow and known as reverse-bias pn junction leakage current (I_1). Sub threshold or weak inversion conduction current between source and drain in an MOS transistor occurs when gate

voltage is driven below the threshold voltage (V_{th}) and called as Sub Threshold leakage Current (I_2). Reduction of gate oxide thickness results in an increase in the field across the oxide. The high electric field coupled with low oxide thickness results in tunneling of electrons from substrate to gate leads to Gate oxide tunneling current (I_3). In a short-channel transistor, due to high electric field near the S_i-S_iO_2 interface, electrons or holes can gain sufficient energy from the electric field to cross the interface potential barrier and enter into the oxide layer. This effect is known as hot-carrier injection and responsible for gate current to flow (I_4). Gate Induced Drain Leakage (GIDL) is due to high field effect in the drain junction of an MOS transistor. When the gate is biased to form an accumulation layer at the silicon surface, the silicon surface under the gate has almost same potential as the p-type substrate which leads to a current flow (I_5). Punch through in a MOSFET is an extreme case of channel length modulation where the depletion layers around the drain and source regions merge into a single depletion region. The field underneath the gate then becomes strongly dependent on the drain-source voltage, as is the drain current. Punch through causes a rapidly increasing current (I_6) with increasing drain-source voltage. This effect is undesirable as it increases the output conductance and limits the maximum operating voltage of the device. Currents.I_2, I_5 and I_6 and are off-state leakage mechanisms, while I1 and I_3 occur in both ON and OFF states. I_4can occur in the off state, but more typically occurs during the transistor bias states in transition[3].

In Nano CMOS circuits, Sub-threshold and Gate Leakage currents are proven as the dominant factors in deciding the Static Power and contribute significantly to overall power consumption. Among these two components, Gate Leakage is mainly due to electron tunneling through thin gate oxide layer from gate to substrate. But sub-threshold leakage is caused by many factors which must be look into particularly in CMOS circuits employed in portable applications to reduce the power dissipation considerably.

Subthreshold or weak inversion conduction current between source and drain in a MOS transistor occurs when gate voltage is below the transistor threshold voltage(V_{th}). The Subthreshold or weak inversion current(I_{ds}) can be expressed as:

$$I_{ds} = \mu_0 C_{ox} \frac{W}{L} (m-1)(v_T)^2 e^{\frac{(v_g - V_{th})}{m v_T}} \left(1 - e^{\frac{-v_{ds}}{v_T}}\right) \quad (5)$$

Where $m = 1 + \frac{C_{dm}}{C_{ox}} = 1 + \frac{\frac{\varepsilon_{si}}{W_{dm}}}{\frac{\varepsilon_{ox}}{t_{ox}}}$ (6)

and V_{th} is threshold voltage and $v_T = \frac{kT}{q}$ is the thermal voltage. C_{ox} is the gate oxide capacitance, μ_0 is the zero bias mobility and m is the body effect coefficient. W_{dm} is the maximum depiction layer width and t_{ox} is the gate oxide thickness. C_{dm} is the capacitance of the depletion layer. Reverse biasing well to source junction of a MOSFET widens the bulk depletion region and increases the threshold voltage(V_{th}). The effect of body bias can be considered in the threshold voltage equation and is

$$V_{th} = V_{fb} + 2\psi_B + \frac{\sqrt{2\varepsilon_{si} q N_a (2\psi_B + V_{bs})}}{C_{ox}} \quad (7)$$

Where V_{fb} is the flat band voltage, N_a is the doping density in the substrate and $\psi_B = \left(\frac{kT}{q}\right) ln \frac{N_a}{n_i}$ is the difference between the Fermi potential and the intrinsic potential in the substrate and n_i is the intrinsic carrier concentration.

Finally the subthreshold leakage of a MOS device including weak inversion, DIBL and body effect can be modeled as:

$$I_{sub} = A e^{\frac{1}{m v_T}(V_G - V_s - V_{tho} - \gamma' V_s + \eta V_{ds})} \left(1 - e^{\frac{-V_{ds}}{v_T}}\right) \quad (8)$$

Where $A = \mu_0 C'_{ox} \frac{W}{L_{eff}} (v_T)^2 e^{1.8} e^{\frac{-dV_{th}}{\eta v_T}}$ (9)

Sub-threshold leakage current (I_{sub}) is also computed using another equation:

$$I_{sub} = I_0 \left[1 - exp\left(-\frac{V_{ds}}{v_t}\right)\right] exp\left[\frac{V_{gs} - V_{th} - V'_{off}}{\eta v_t}\right] \quad (10)$$

Where $I_0 = \mu \frac{W}{L} \sqrt{\frac{q\varepsilon_{si} N_{dep}}{2\Phi_s}} v_t^2$ (11)

V_{ds} is the drain to source voltage, V_t is thermal voltage and equal to K_BT/q, V_{th} is the threshold voltage, V'_{off} is the offset voltage = V_{off} + V_{offL}/L_{eff} which determines the channel current at V_{gs} = 0, n is the sub-threshold swing parameter. μ, W, L are mobility, Width and Length of the transistor respectively. N_{dep} is the substrate doping concentration at depletion edge at V_{bs} = 0, where V_{bs} is bulk to source potential. q, ε_{si}, $\boldsymbol{\Phi}_s$ are intrinsic charge carrier, permittivity of silicon and surface charge potential respectively[4-5].

Many techniques are proposed by as many researchers in controlling the sub-threshold current particularly in nano-meter regime as it is the dominant factor in deciding the overall power consumption of the circuits by pushing dynamic power behind. Generally these techniques are classified as active and standby mode techniques at circuit level.

3. BRIEF REVIEW OF LEAKAGE CURRENT REDUCTION TECHNIQUES

For a CMOS circuit, the total power dissipation includes dynamic and static components during the active mode of operation. In the standby mode, the power dissipation is due to the standby leakage current. Dynamic power dissipation consists of two components. One is the switching power due to charging and discharging of load capacitance. The other is short circuit power due to the nonzero rise and fall time of input waveforms. The static power of a CMOS circuit is determined by the leakage current through each transistor [6].

Hence, to suppress the power consumption in low-voltage circuits, it is necessary to reduce the leakage power in both the active and standby modes of operation. The reduction in leakage current has to be achieved using both process- and circuit-level techniques. Standby leakage current is the current wasted when the circuit is in idle state while the active leakage current flows when the circuit is in use. At the device level, leakage current can be suppressed by controlling the doping concentration and profile of the semiconductor and carefully changing the physical dimension of transistors. Whereas at the circuit level, leakage current is being effectively kept under control by employing multiple threshold transistors and adopting different biasing schemes for the MOSFETS used in the circuit [7-9]. Some of the already proposed circuit level leakage current reduction techniques are i) Multi V_{th} Technique (MTCMOS)[7-8], ii) Super Cut-off CMOS (SCCMOS)[9-10], iii) Dual Threshold Voltage technique (DTCMOS)[11], iv) Variable V_{th} technique (VTCMOS)[12], v) Dynamic V_{th} Technique [13-14], vi) Forced Transistor Stacking (FTS)[15-16], vii) Sleepy Stack Transistor insertion Technique (SS)[17-18], viii) Adaptive Body Bias Scheme (ABB)[19-20] and ix) Input Vector Control Technique (IVC)[21]. Whereas at the device level, works were reported previously related to transform the fabrication platform from bulk technology to Silicon On Insulator (SOI) technology, Separation by Implantation of Oxygen (SIMOX) and fabricating novel devices such as Double Gate MOSFET and FinFET.

There are two approaches in leakage current reduction of CMOS circuits. With Standby mode techniques, circuit is disconnected from the supply and ground rails with the help of sleep transistors. Sleep transistors creates virtual supply and virtual ground rails for the CMOS circuits to operate in normal conditions. In active mode techniques, additional transistors are introduced at suitable places in conventional circuits such as transistor stack to reduce leakage current.

3.1 Standby Mode Techniques

3.1.1 Multithreshold CMOS Technique (MTCMOS)

In this technique, a sleep transistor with high threshold voltage is inserted in series between the circuit and power rails. It provides high performance during active mode and saves leakage power during standby mode by providing power gating. During standby mode, the sleep transistors are made 'off' and the CMOS logic circuit is disconnected from the power rails. During active mode, the sleep transistors are turned ON and normal operation of circuit resumes.

3.1.2 Super Cutoff CMOS Technique (SCCMOS)

This technique is very much similar to the MTCMOS but instead of a high V_{th} sleep transistor, a nominal V_{th} sleep transistor is employed to reduce the additional delay caused due to the presence of increased threshold value in sleep transistor.

3.2 Active Mode Techniques

3.2.1 Forced Transistor Stacking Technique (FTS)

In this technique a single transistor of width 'W' is replaced by two transistors each of width '$\frac{W}{2}$'. This is called as stacking and this effect helps in reducing the leakage current, when multiple transistors are connected in series and one or few of them are turned off. This happens due to the following situations with respect to a stacked arrangement of NMOS network. *(i)* Due to positive source potential V_m in the intermediate node of stacked transistors Q1 and Q2 of Figure 2, gate-to-source voltage of stacked transistor becomes negative, so the sub threshold current reduces greatly. *(ii)* Due to $V_m>0$, body -to-source potential of stacked transistor decreases resulting in increasing threshold voltage and thus reducing sub threshold leakage. *(iii)* Due to $V_m>0$,drain -to-source potential of stacked transistor decreases resulting in increasing threshold voltage and thus reducing sub threshold leakage.

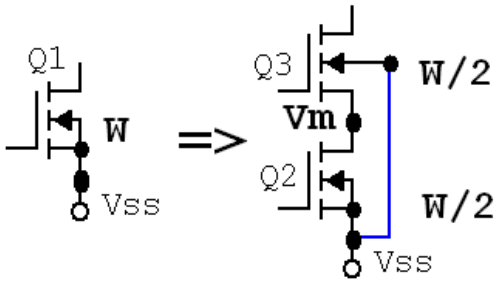

Fig 2: Illustration of stacking effect

3.2.2 Sleepy Stack Technique (SS)

In this technique, Forced Transistor Stacking (FTS) is first implemented. Then to one of the stacked transistors, a sleep transistor is inserted in parallel. Leakage power is suppressed by the parallel connected sleep, high V_{th} transistors. 'Off' transistors in the stack, induce stack effect that reduces leakage power

4. EXPERIMENTAL SET UP

As Delay Flip-Flop(DFF) has been the integral part of any digital system to construct the sequentail part of it. This paper aims at anlaysing the performance of different architectures of DFF with respect to performance metrics such as average power, leakage power, delay and Power Delay Product(PDP). Two architectures with True Single Phase Clocking(TSPC) has been considered with 8 and 9 transistors(Figures 3 and 4) respectively and a conventional 32T CMOS NAND based DFF (Figure 5) is also considered for anlaysis and comparison of the above performance metrics.

All the circuits are designed using 16nm Berkley's Predictive Technology Model Files [34-35] considering High K dielectric, Metal Gate, Strained silicon, Silicon on Insulator (SOI) technology. High-K gate dielectric can be modeled as SiO_2 (relative permittivity: 3.9) with an equivalent SiO_2 thickness. For example, 3nm gate dielectric with a dielectric constant of 7.8 would have an equivalent oxide thickness of 1.5nm. Since all the parameters are derived using Berkley Short Channel Insulated Gate FET simulation model, the simulated results are expected to be very close to actual results. Tanner SPICE is used for simulation of output waveforms and power estimation.

a) 8T-TSPC architecture

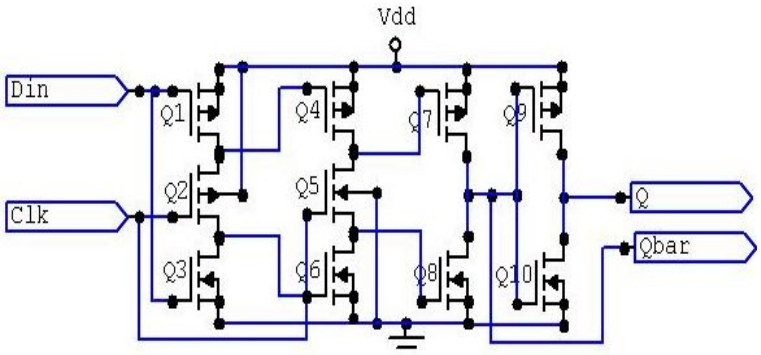

Fig 3: 8T-TSPC CMOS architecture

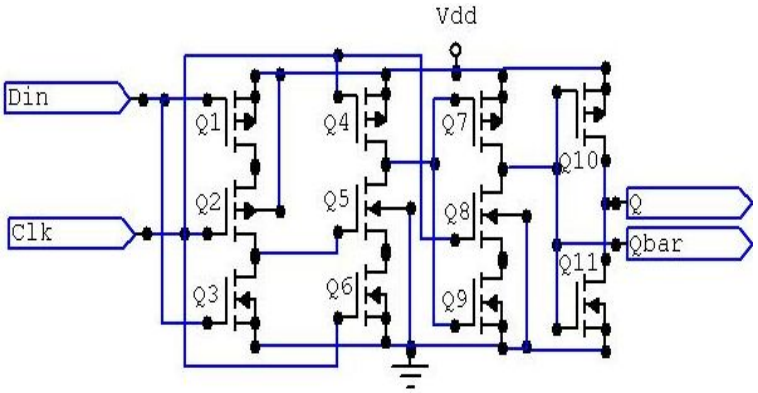

Fig 4: 9T-TSPC CMOS architecture

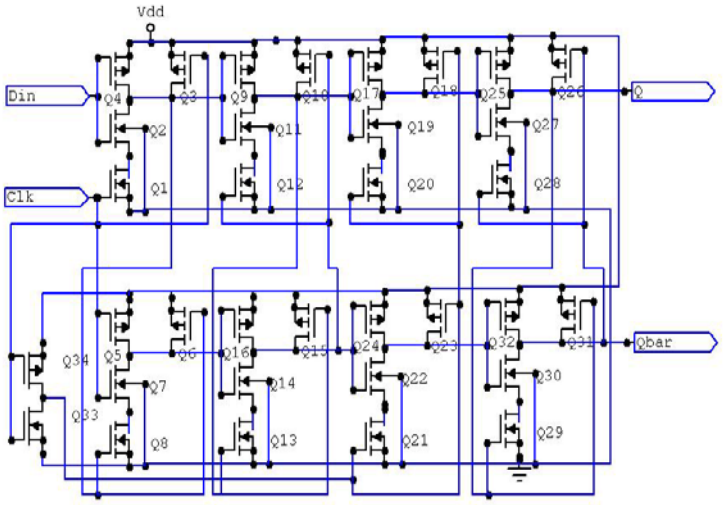

Fig 5: CMOS NAND based DFF architecture

5. RESULTS AND DISCUSSION

Table 1: Performance analysis of 8TTSPC DFF architecture

Circuit Description	P_{avg} (nW)	$P_{standby}$ (nW)	P_{leak} (nW)	Delay (ns)	Power Delay Product (fJ)	% Reduction	
						P_{avg}	P_{leak}
Base Case	5.08	-	0.415	15.29	77.67	--	--
MTCMOS	3.92	3.9	0.004	09.25	36.26	22.83	99.03
SCCMOS	3.46	4.2	0.005	10.92	45.53	31.89	98.79
FTS	2.15	-	0.256	27.19	102.77	57.67	38.31
SS	1.60	1.9	0.256	12.09	21.52	68.50	38.31

Table 2: Performance analysis of 9TTSPC DFF architecture

Circuit Description	P_{avg} (nW)	$P_{standby}$ (nW)	P_{leak} (nW)	Delay (ns)	Power Delay Product (fJ)	% Reduction	
						P_{avg}	P_{leak}
Base Case	3.51	-	18.08	2.125	07.458	--	--
MTCMOS	2.06	2.06	0.005	5.45	11.227	41.31	99.99
SCCMOS	2.52	2.73	0.285	3.18	08.014	28.20	98.42
FTS	2.26	-	15.79	1.7	03.842	35.61	12.6
SS	2.11	3.47	15.80	1.76	3.7136	39.88	12.6

Table 3: Performance analysis of CMOS NAND based DFF architecture

Circuit Description	P_{avg} (nW)	$P_{standby}$ (nW)	P_{leak} (nW)	Delay (ns)	Power Delay Product (fJ)	% Reduction	
						P_{avg}	P_{leak}
Base Case	8.85	-	1.377	0.74	05.28	--	--
MTCMOS	7.65	0.13	0.011	4.80	20.41	13.6	99.20
SCCMOS	7.25	0.12	0.011	3.91	18.05	18.1	99.20
FTS	8.06	-	1.228	1.12	07.72	08.9	10.82
SS	7.57	7.00	1.228	1.61	09.89	14.5	10.82

Table 4: Comparison of percentage of Power reduction among various architectures

Circuit Description	% Reduction (compared to base case)					
	P_{avg}			P_{leak}		
	8TTSPC	9TTSPC	NAND based DFF	8TTSPC	9TTSPC	NAND based DFF
MTCMOS	22.83	41.31	13.6	99.03	99.99	99.20
SCCMOS	31.89	28.20	18.1	98.79	98.42	99.20
FTS	57.67	35.61	08.9	38.31	12.6	10.82
SS	68.50	39.88	14.5	38.31	12.6	10.82

From the results, it is observed from Table 1 that for 8T-TSPC circuit, Sleepy Stack technique produces better result of 68.50% power reduction when compared to base case for P_{avg} , but MTCMOS Technique reports the highest power saving of 99.20% for leakage power P_{leak}. Power Delay Product is also minimum for sleepy stack technique. From Table 2, it is observed that, employing MTCMOS Technique produces the optimum values for 9T-TSPC circuit in case of P_{avg} (41.3%) and P_{leak} (99.99). But PDP is reported with minimum value in the case of Sleepy Stack reduction technique. Results from Table 3 indicates that SCCMOS Technique is better suited for a NAND based DFF architecture which produces the highest percentage of power reduction for both P_{avg} (18.1)

and P_{leak} (99.20) where the PDP is low for conventional architecture. In Table 4 the percentage of power reductions are given in a consolidated format. From the results, it is observed that, 8T-TSPC architecture has the better percentage of average power reduction for 3 cases (SSCMOS, FTS and SS) and also in the case of leakage power reduction, 8T-TSPC has better results for 2 techniques (FTS and SS).

5. CONCLUSION

In this paper, performance analyses of different D-Flip-flop Circuits are presented. Efficiency of Power reduction varies with different topology with different technique. Best average power reduction (68.50%) is reported with sleepy stack technique, where as for leakage power MTCMOS technique produces the best result (99.99) due to its power gating ability. Lowest Power Delay Product value (3.7136 femto Joules) is reported with 9T-TSPC architecture.

ACKNOWLEDGEMENTS

Authors thank the SKCT management and acknowledge the immense help received from the scholars whose articles are cited and included in references of this manuscript. The authors are also grateful to authors / editors / publishers of all those articles, journals and books from where the literature for this article has been reviewed and discussed.

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