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Power Quality Enhancement Using VSC Based DSTATCOM

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ABSTRACT

In this paper, a new three-phase four-wire distribution static compensator (DSTATCOM) based on a T-connected transformer and a three-leg voltage source converter (VSC) is proposed for power quality improvement. The T-connected transformer connection mitigates the neutral current and the three-leg VSC compensates harmonic current, reactive power, and balances the load. Two single-phase transformers are connected in T-configuration for interfacing to a three-phase four-wire power distribution system and the required rating of the VSC is reduced. The insulated gate bipolar transistor (IGBT) based VSC is supported by a capacitor and is controlled for the required compensation of the load current. The dc bus voltage of the VSC is regulated during varying load conditions. The DSTATCOM is tested for power factor correction and voltage regulation along with neutral current compensation, harmonic elimination, and balancing of linear loads as well as nonlinear loads. The performance of the three-phase four-wire DSTATCOM is validated using MATLAB software with Simulink.

Keywords: *CPDs, DSTATCOM, IGBT and VSC.*

1. INTRODUCTION

Three-Phase four-wire distribution systems are facing severe power quality problems such as poor voltage regulation, high reactive power and harmonics current burden, load unbalancing, excessive neutral current, etc (A.Ghosh and G. Ledwich, 2002) - (Ewald F. Fuchs and Mohammad A. S. Mausoum, 2008). Three-phase four-wire distribution systems are used in commercial buildings, office buildings, hospitals, etc. Most of the loads in these locations are nonlinear loads and are mostly unbalanced loads in the distribution system. This creates excessive neutral current both of fundamental and harmonic frequency and the neutral conductor gets overloaded. The voltage regulation is also poor in the distribution system due to the unplanned expansion and the installation of different types of loads in the existing distribution system. In order to control the power quality problems, many standards are proposed, such as the IEEE-519 standard. There are mitigation techniques for power quality problems in the distribution system and the groups of devices are known by the generic name of custom power devices (CPDs) (A.Ghosh and G. Ledwich, 2002). The distribution static compensator (DSTATCOM) is a shunt-connected CPD capable of compensating power quality problems in the load current. Some of the topologies of DSTATCOM for three phase four-wire system for the mitigation of neutral current along with power quality compensation in the source current are four-leg voltage source converter (VSC), three single-phase VSCs, three-leg VSC with split capacitors, three-leg VSC with zig-zag transformer(Hurng- Liahng Jou et al., 2005) - (Hurng-Liahng, Kuen et al., 2008), and three-leg VSC with neutral terminal at the positive or negative of dc bus (H.L.Jou, et al., 2008). The voltage regulation in the distribution feeder is improved by installing a shunt compensator. There are many control schemes reported in the literature for control of shunt active compensators such as instantaneous reactive power theory, power balance theory, synchronous reference frame theory, etc. The synchronous reference frame theory is used for the control of the proposed DSTATCOM.

2. SYSTEM CONFIGURATION AND DESIGN

Fig. 1 shows the single-line diagram of the shunt-connected DSTATCOM based distribution system. The dc capacitor connected at the dc bus of the converter acts as an energy buffer and establishes a dc voltage for the normal operation of the DSTATCOM system. The DSTATCOM can be operated for reactive power compensation for power factor correction or voltage regulation.

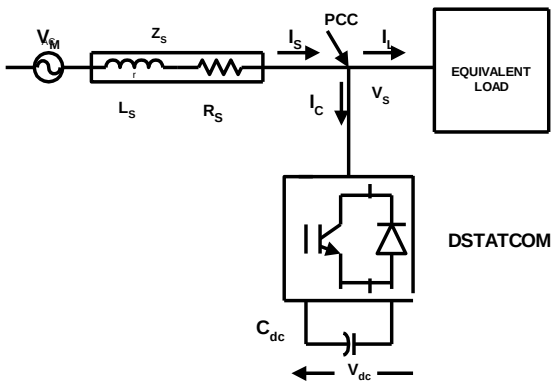

Fig. 1. Single -line diagram of DSTATCOM system

The proposed DSTATCOM consisting of a three-leg VSC and a T-connected transformer is shown in Fig.2, where the T-connected transformer is responsible for neutral current compensation.

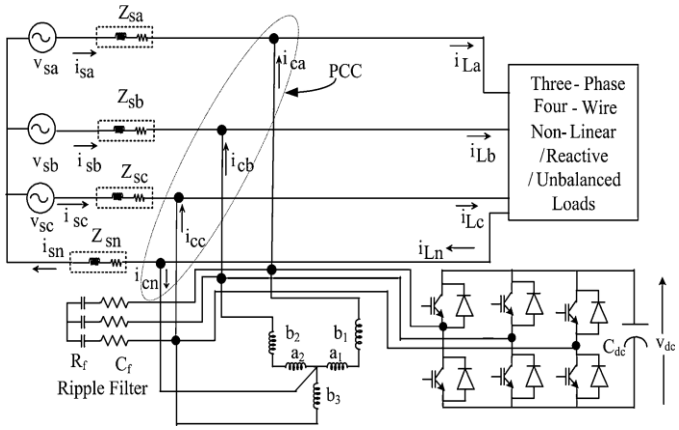

Fig.2. Schematics of the proposed three-leg VSC with T-connected transformer based DSTATCOM connected in distribution system.

A three-leg VSC is used as an active shunt compensator along with a star-connected transformer, as shown in Fig.1 and this topology has six IGBTs, three ac inductors and one dc capacitor. The required compensation to be provided by the DSTATCOM decides the rating of the VSC components.

2.1 DC Capacitor Voltage

The minimum dc bus voltage of VSC of DSTATCOM should be greater than twice the peak of the phase voltage of the system (B. N. Singh, et al., 2004). The dc bus voltage is calculated as

$$V_{dc} = \frac{2\sqrt{2}V_{LL}}{\sqrt{3}m} \quad (1)$$

Where m is the modulation index and is considered as 1 and V_{LL} is the ac line output voltage of DSTATCOM. Thus, Vdc is obtained as 677.69 V for V_{LL} of 415 V and is selected as 700 V.

2.2 DC Bus Capacitor

The value of dc capacitor (C_{dc}) of VSC of DSTATCOM depends on the instantaneous energy available to the DSTATCOM during transients (B. N. Singh, et al., 2004). The principle of energy conservation is applied as

$$\frac{1}{2}C_{dc}[(V_{dc}^2)-(V_{dc1}^2)] = 3V(aI)t \quad (2)$$

where V_{dc} is the reference dc voltage and V_{dc1} is the minimum voltage level of dc bus, a is the overloading factor, V is the phase voltage, I is the phase current, and t is the time by which the dc bus voltage is to be recovered.

Considering the minimum voltage level of the dc bus, V_{dc1} = 690V, V_{dc} = 700V, V = 239.60V, I = 27.82A, t = 350µs, a = 1.2. The calculated value of C_{dc} is 2600µF and is selected as 3000µF.

2.3 AC Inductor

The selection of the ac inductance (L_f) of VSC depends on the current ripple $i_{cr(p-p)}$, switching frequency f_s, dc bus voltage (V_{dc}), and L_f is given as (B. N. Singh, et al., 2004)

$$L_f = \frac{\sqrt{3}mV_{dc}}{12af_s i_{cr(p-p)}} \quad (3)$$

where m is the modulation index and a is the overload factor. Considering, $i_{cr(p-p)}$ =5%, f_s = 10kHz, m = 1, V_{dc} = 700 V, a = 1.2. The L_f value is calculated to be 2.44 mH. A round-off value of L_f of 2.5 mH is selected in this investigation.

2.4 Ripple Filter

A low-pass first-order filter tuned at half the switching frequency is used to filter the high-frequency noise from the voltage at the PCC. Considering a low impedance of 8.1 Ω for the harmonic voltage at a frequency of 5 kHz, the ripple filter capacitor is designed as C_f = 5µF. A series resistance (R_f) of 5Ω is included in series with the capacitor (C_f). The impedance is found to be 637 Ω at fundamental frequency, which is sufficiently large, and hence, the ripple filter draws negligible fundamental current.

3. CONTROL OF DSTATCOM

The control approaches available for the generation of reference source currents for the control of VSC of DSTATCOM for three-phase four-wire system are instantaneous reactive power theory (IRPT), synchronous reference frame theory (SRFT), unity power factor (UPF) based, instantaneous symmetrical components based, etc. The SRFT is used in this investigation for the control of the DSTATCOM. A block diagram of the control scheme is shown in Fig. 3.

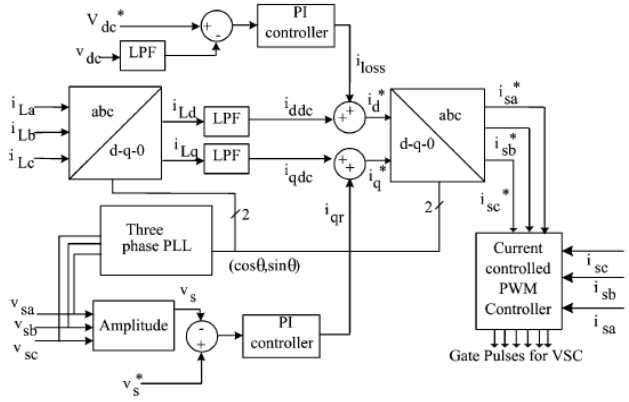

Fig.3. Control scheme for the three-leg-VSC-based DSTATCOM in three phases four wire system.

The load currents (i_{La}, i_{Lb}, i_{Lc}), the PCC voltages (V_{Sa},V_{Sb}, V_{Sc}), and dc bus voltage (V_{dc}) of DSTATCOM are sensed as feedback signals. The load currents from the *a–b–c* frame are first converted to the *α–β–o* frame and then to the *d–q–o* frame using

$$\begin{bmatrix} i_{Lq} \\ i_{Ld} \\ i_{Lo} \end{bmatrix} = \begin{bmatrix} \cos\theta & \cos(\theta-\frac{2\pi}{3}) & \cos(\theta+\frac{2\pi}{3}) \\ \sin\theta & \sin(\theta-\frac{2\pi}{3}) & \sin(\theta+\frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (4)$$

where cos θ and sin θ are obtained using a three-phase phase locked loop (PLL). A PLL signal is obtained from terminal voltages for generation of fundamental unit vectors (S. Bhattacharya and D. Diwan, 1995) for conversion of sensed currents to the *d–q–o* reference frame. The SRF controller extracts dc quantities by a low-pass filter, and hence, the non-dc quantities (harmonics) are separated from the reference signal. The *d*-axis and *q*-axis currents consist of fundamental and harmonic components as

$$i_{Ld} = i_{d\,dc} + i_{d\,ac} \quad (5)$$

$$i_{Lq} = i_{q\,dc} + i_{q\,ac} \quad (6)$$

3.1 UPF Operation of DSTATCOM

The control strategy for reactive power compensation for UPF operation considers that the source must deliver the mean value of the direct-axis component of the load current along with the active power component current for maintaining the dc bus and meeting the losses (i_{loss}) in DSTATCOM. The output of the proportional-integral (PI) controller at the dc bus voltage of DSTATCOM is considered as the current (i_{loss}) for meeting its losses.

$$i_{loss(n)} = i_{loss(n-1)} + K_{pd}(V_{de(n)} - V_{de(n-1)}) + K_{id}V_{de(n)} \quad (7)$$

where $V_{de}(n) = V^*_{dc} - V_{dc(n)}$ is the error between the reference V^*_{dc} and sensed V_{dc} voltages at the *n*th sampling instant. K_{pd} and K_{id} are the proportional and integral gains of the dc bus voltage PI controller.

The reference source current is therefore

$$i^*_d = i_{d\,dc} + i_{loss}\,. \quad (8)$$

The reference source current must be in phase with the voltage at the PCC but with no zero-sequence component. It is therefore obtained by the following reverse Park's transformation with i^*_d as in (8) and i^*_q as in (12) and i^*_0.

$$\begin{bmatrix} i^*_a \\ i^*_b \\ i^*_c \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 1 \\ \cos(\theta-\frac{2\pi}{3}) & \sin(\theta-\frac{2\pi}{3}) & 1 \\ \cos(\theta+\frac{2\pi}{3}) & \sin(\theta+\frac{2\pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} i^*_d \\ i^*_q \\ i^*_o \end{bmatrix} \quad (9)$$

3.2 Zero-Voltage Regulation (ZVR) Operation of DSTATCOM

The compensating strategy for ZVR operation considers that the source must deliver the same direct-axis component $i_d{}^*_{dc}$, as mentioned in (8) along with the sum of quadrature-axis current ($i_{q\,dc}$) and the component obtained from the PI controller (i_{qr}) used for regulating the voltage at PCC. The amplitude of ac terminal voltage (V_s) at the PCC is controlled to its reference voltage using the PI controller. The output of PI controller is considered as the reactive component of current (i_{qr}) for zero-voltage regulation of ac voltage at PCC. The amplitude of ac voltage (V_S) at PCC is calculated from the ac voltages (V_{sa}, V_{sb}, V_{sc}) as

$$V_s = (2/3)^{1/2}(V_{sa}^2 + V_{sb}^2 + V_{sc}^2)^{1/2} \quad (10)$$

Then, a PI controller is used to regulate this voltage to a reference value as

$$i_{qr(n)} = i_{qr(n-1)} + K_{pq}(V_{te(n)} - V_{te(n-1)}) + K_{iq}V_{te(n)} \quad (11)$$

where $V_{te(n)} = V^*_S - V_{S(n)}$ denotes the error between reference (V^*_S) and actual ($V_{S(n)}$) terminal voltage amplitudes at the *n*th sampling instant. K_{pq} and K_{iq} are the proportional and integral gains of the dc bus voltage PI controller. The reference source quadrature-axis current is

$$i^*_q = i_{qdc} + i_{qr} \quad (12)$$

The reference source current is obtained by reverse Park's transformation using (10) with i^*_d as in (8) and i^*_q as in (12) and i^*_0 as zero.

3.3 Computation of Controller Gains

The gains of the controllers are obtained using the Ziegler –Nichols step response technique. The gains of the controller are computed using the following equations:

$$K_p = 1.2U/GT \quad (13)$$

$$K_i = 0.6U/GT^2 \quad (14)$$

Where U= step input of amplitude, G= maximum gradient, T= the point at which the line of maximum gradient crosses the time axis.

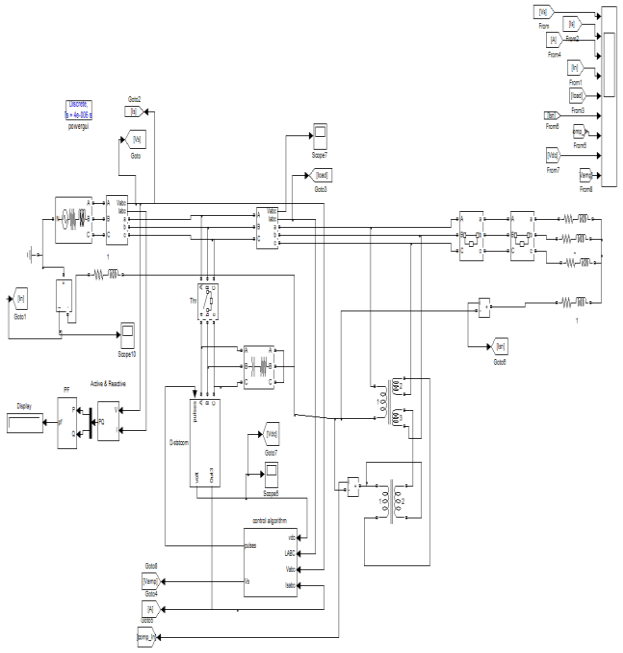

Figure 4. MATLAB model of the T-connected transformer and the three-leg-VSC-based DSTATCOM connected system

3.4 Current-Controlled Pulse Width Modulation (PWM) Generator

In a current controller, the sensed and reference source currents are compared and a proportional controller is used for amplifying current error in each phase before comparing with a triangular carrier signal to generate the gating signals for six IGBT switches of VSC of DSTATCOM.

4. MODELING AND SIMULATION

The three-leg VSC and the Star-connected-transformer-based DSTATCOM connected to a three-phase four-wire system is modeled and simulated using the MATLAB with its Simulink and PSBs. The ripple filter is connected to the DSTATCOM for filtering the ripple in the PCC voltage. The MATLAB-based model of the three-phase four-wire DSTATCOM is shown in Fig. 4. The Star -connected transformer in parallel to the load, the three-phase source, and the shunt-connected three-leg VSC are connected as shown in Fig. 4. The available model of linear transformers, which includes losses, is used for modeling the Star-connected transformer. The control algorithm for the DSTATCOM is also modeled in MATLAB. The reference source currents are derived from the sensed PCC voltages (V_{sa}, V_{sb},V_{sc}), load currents (i_{La}, i_{Lb}, i_{Lc}), and the dc bus voltage of DSTATCOM (V_{dc}). A PWM current controller is used over the reference and sensed source currents to generate the gating signals for the IGBTs of the VSC of the DSTATCOM.

5. RESULTS AND DISCUSSION

The performance of the T-connected transformer and three-leg VSC based three-phase four-wire DSTATCOM is demonstrated for power factor correction and voltage regulation along with harmonic reduction, load balancing, and neutral current compensation. The developed model is analyzed under varying loads and the results are discussed below.

5.1 Performance of DSTATCOM with Linear Load for Neutral Current Compensation, Load Balancing, and ZVR Operation

The dynamic performance of the DSTATCOM under linear lagging power factor unbalanced load condition is shown in fig.5. At 0.2s, the load is changed to two-phase load and to single-phase load at 0.3s. The PCC voltages (V_s), source currents (i_s), load currents (i_L), compensator currents (i_C), source neutral current (i_{Sn}), load-neutral current (i_{Ln}), compensator neutral current (i_{Cn}), dc bus voltage (V_{dc}), and amplitude of voltage (V_s) at PCC are also shown. The source neutral current is observed as nearly zero, and this verifies the proper compensation. It is also observed that the dc bus voltage of DSTATCOM is able to maintain close to the reference value under all disturbances. The amplitude of PCC voltage is maintained at the reference value under various load disturbances, which shows the ZVR mode of operation of DSTATCOM.

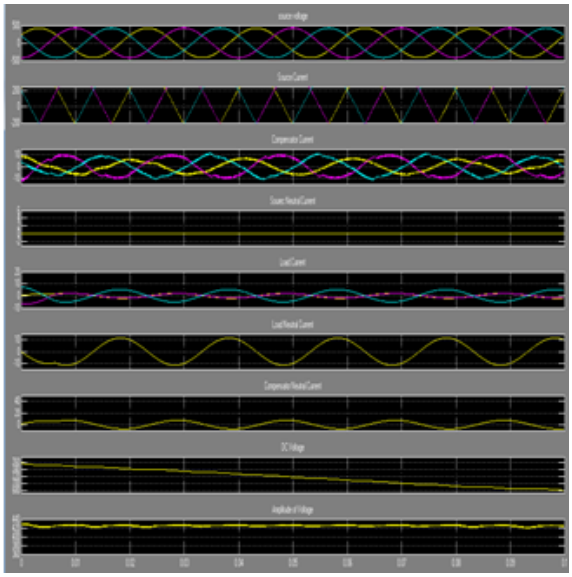

Figure 5. Performance of DSTATCOM with Linear Load for Neutral Current Compensation, Load Balancing, and ZVR operation

5.2 Performance of DSTATCOM with Linear Load for Neutral Current Compensation, Load Balancing, and UPF Operation

The dynamic performance of the DSTATCOM during linear lagging power-factor-unbalanced load condition is depicted in the fig.6. At 0.2s, the load is changed to two-phase load and to single-phase load at 0.3s. The PCC voltages (V_S), source currents (i_s), load currents (i_L), compensator currents (i_C), source-neutral current (i_{Sn}), load-neutral current (i_{Ln}), compensator-neutral current

(i_{Cn}), dc bus voltage (V_{dc}), and amplitude of voltage (V_S) at PCC are also depicted. The reactive power is compensated for power factor correction, and the source currents are balanced and sinusoidal. The source-neutral current is nearly zero and it verifies the proper compensation. It is also observed that the dc bus voltage of DSTATCOM is maintained at the reference value under all load disturbances.

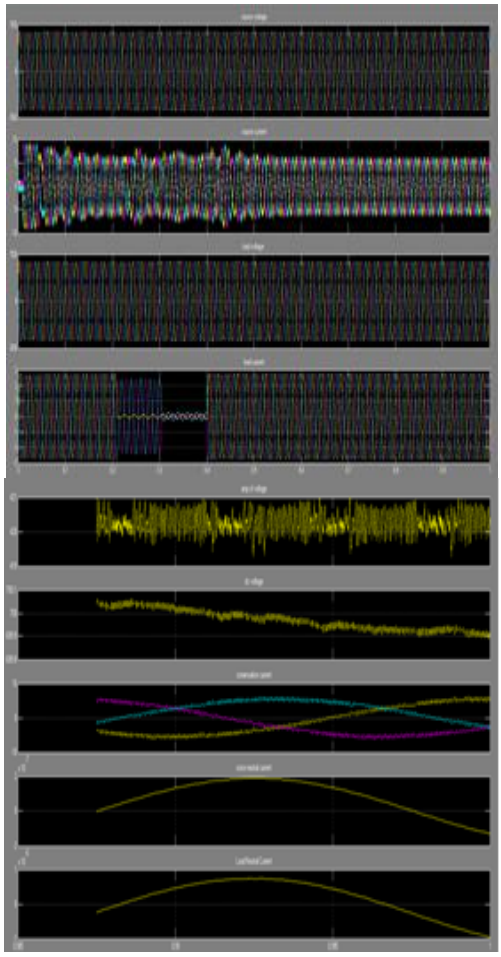

Figure 6. Performance of DSTATCOM with Linear Load for Neutral Current Compensation, Load Balancing, and UPF Operation

5.3 Performance of DSTATCOM with Non-Linear Load for Harmonic compensation, Load Balancing, and ZVR Operation

The dynamic performance of the DSTATCOM with nonlinear and unbalanced load is shown in fig 7. It is observed that the harmonic current is compensated and the source currents are balanced and sinusoidal. At 0.2s, the load is changed to two-phase load and to single-phase load at 0.3s. The source currents are still balanced and sinusoidal even when the load current in a phase is zero. The dc bus voltage of DSTATCOM is maintained at nearly its reference value under all load disturbances. The amplitude of PCC voltage is maintained at the reference value under various load disturbances, which shows the ZVR mode of operation of DSTATCOM.

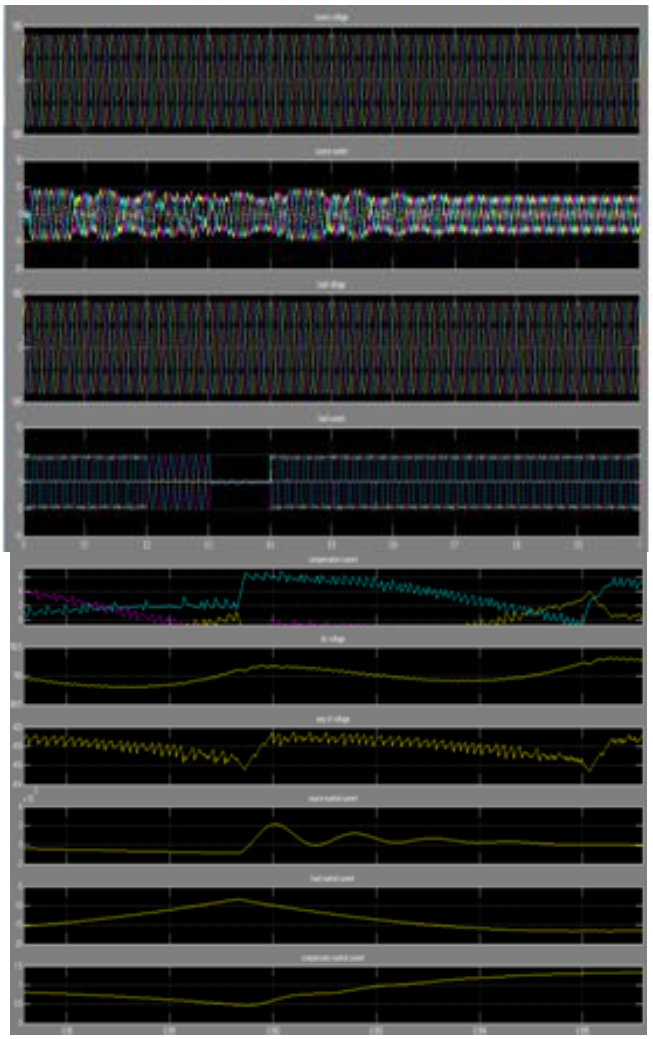

Figure 7. Performance of DSTATCOM with Non-Linear Load for Harmonic compensation, Load Balancing, and ZVR Operation

5.4 Performance of DSTATCOM with Nonlinear Load for Harmonic Compensation, Load Balancing, and UPF Operation

The dynamic performance of the DSTATCOM during nonlinear unbalanced load condition is shown in fig 8. The source currents are observed as balanced and sinusoidal under all these conditions. At 0.2s, the load is changed to two-phase load and again to single-phase load at 0.3s. The PCC voltages (V_S), source currents (i_S), load currents (i_{La}, i_{Lb}, i_{Lc}), compensator currents (i_C), source-neutral current (i_{Sn}), compensator-neutral current (i_{Cn}), load-neutral current (i_{Ln}), dc bus voltage (V_{dc}), and amplitude of voltage (V_S) at PCC are also depicted. The dc bus voltage of DSTATCOM is maintained at the reference value under all load disturbances through proper control. This shows

the satisfactory performance of DSTATCOM for harmonic compensation as stipulated by the IEEE-519 standard.

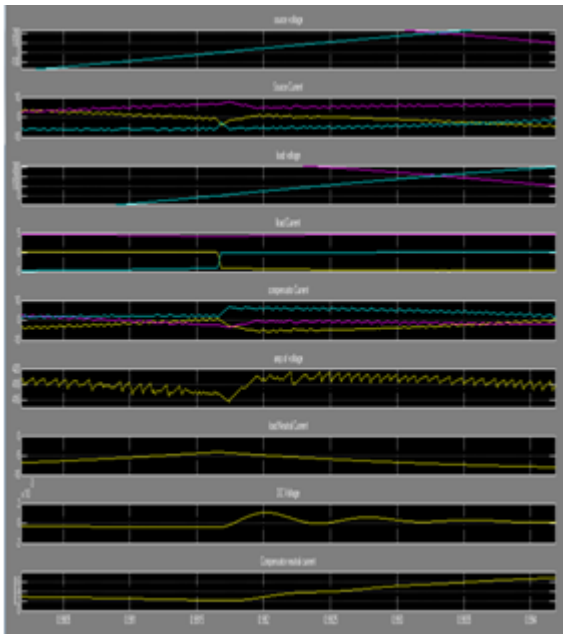

Figure 8. Performance of DSTATCOM with Non-Linear Load for Harmonic compensation, Load Balancing, and UPF Operation

6. CONCLUSION

The performance of a new topology proposed has been demonstrated for neutral current compensation along with reactive power compensation, harmonic elimination, and load balancing. The T-connected transformer has mitigated the source-neutral current. The dc bus voltage of the DSTATCOM has been regulated to the reference dc bus voltage under all varying loads. Two single phase transformers are used for the Star-configuration of the transformer to interface with a three-phase four-wire system. The total KVA rating of the Star-connected transformer is lower than a star/delta transformer for a given neutral current compensation. The experimental results on a prototype have verified that the Star-connected transformer has been effective in compensating the zero sequence fundamental and harmonics currents. In this paper, two single phase transformers are connected in T-configuration for interfacing to a three-phase four-wire power distribution system. So some winding losses and cost of winding for required values will be more. If we replace the T-connected transformer with one three-phase transformer, then winding losses will be less and also cost of the winding will be less. So the Star connected transformer also will be useful to compensate the neutral current in the distribution system.

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