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# Investigations on Three Phase Five Level Flying Capacitor Multilevel Inverter

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## ABSTRACT

The use of multilevel inverters is widespread in medium voltage applications due to their inherent voltage sharing among the devices. This work proposes three phase five level Flying Capacitor Multilevel Inverter (FCMLI) using various modulating techniques for induction motor load. These Pulse Width Modulating (PWM) techniques include Carrier Overlapping (CO) strategy, Variable Frequency (VF) strategy, Phase Shift (PS) strategy and Sub-Harmonic Pulse Width Modulation (SHPWM) i.e. Phase Disposition (PD) strategy, Phase Opposition Disposition (POD) strategy and Alternate Phase Opposition Disposition (APOD) strategy. The Total Harmonic Distortion (THD), $V_{RMS}$ (fundamental), crest factor, form factor and distortion factor are evaluated for various modulation indices. Simulation is performed using MATLAB-SIMULINK. It is observed that PODPWM method provides output with relatively low distortion. COPWM is also found to perform better since it provides relatively higher fundamental RMS output voltage for Induction Motor (IM) load.

**Keywords:** *CF, FCMLI, FF, PWM , THD, $V_{rms}$*

## LIST OF ABBREVATIONS

| | |
|---|---|
| CF | Crest Factor |
| THD | Total Harmonic Distortion |
| FF | Form Factor |
| PD | Phase Disposition |
| POD | Phase Opposition and Disposition |
| APOD | Alternate Phase Opposition and Disposition |
| VF | Variable Frequency |
| PS | Phase Shift |
| FCMLI | Flying Capacitor Multilevel Inverter |
| SHPWM | Sub Harmonic Pulse Width Modulation |
| NC | No Connection |
| IM | Induction Motor |
| $A_c$ | Amplitude of the Carrier |
| $A_m$ | Amplitude of the Reference |
| $f_m$ | Frequency of the Modulating Signal |
| $f_c$ | Frequency of the Carrier Signal |
| m | Number of Levels |
| $m_a$ | Amplitude Modulation index |
| $m_f$ | Frequency Modulation index |
| $V_{an}$ | Phase Voltage |

## 1. INTRODUCTION

Multilevel inverters offer a number od advantages when compared to the conventional two level inverter. The recent development of new power semiconductor technologies capable of handling higher voltage and current ratings has helped the consolidation of multilevel topologies in medium voltage drives. Janyavula and Saxena [1] made a detailed study on diode clamped multilevel inverter with respect to modulation index and control strategy. Urmila and Subbarayudu [2] also made a detailed study on pulse width modulation techniques. Natchpong et al [3] proposed a 6.6 KV transformer less motor drive using five level diode clamped inverter for

energy saving pumps and blowers. Trabelsi and Brahim [4] developed a power conditioning system based on flying capacitor inverter. Zhang and Sun [5] introduced an efficient control strategy for a five level inverter comprising flying capacitor asymmetrical H-bridge. Mailah et al [6] described in detail simulation and construction of single phase flying capacitor multilevel inveter. Shanthi and Natarajan [7] made a comparative study on carrier overlapping PWM strategies for five level flying capacitor inverter. Huang and Corzine [8] proposed extended operation of flying capacitor multilevel inverters. Lai and Peng [9] made a survey on topologies, controls and applications in multilevel inverter. Kang et al [10] developed a symmetric carrier technique of CRPWM for voltage balance method of flying capacitor multilevel inverter. Kim et al [11] developed a generalized Undeland snubber for flying capacitor multilevel inverter and converter. Mcgrath and Holmes [12] developed sinusoidal PWM of multilevel inverter in the over modulation region. This literature survey reveals few papers only on various PWM techniques and hence this work presents a novel approach for controlling the harmonics of output voltage of chosen MLI fed IM employing sinusoidal switching strategies. Simulations are performed using MATLAB-SIMULINK. Harmonics analysis and evaluation of performance measures for various modulation indices have been carried out and presented.

## 2. MULTILEVEL INVERTER

Multilevel inverter is an effective and practical solution for reducing switching losses in high power inverters. Multilevel inverter concept involves utilizing a higher number of active semiconductor switches to perform the power conversion in small voltage steps for getting higher output voltage and reduction in harmonic distortion. Such multilevel inverter topology permits a significant reduction of the output filter and an improvement of the efficiency greater than 98% for loads greater than 40% of its rated output power. FCMLI is a multiple voltage level inverter topology which uses capacitors (called flying capacitors) for clamping the voltage across the power semiconductor devices. One phase of three phase m level FCMLI requires 2(m-1) semiconductor switches. The five level FCMLI consists of four switching pairs ($S_{A1}$ $S_{A1}$'), ($S_{A2}$ $S_{A2}$'), ($S_{A3}$ $S_{A3}$') and ($S_{A4}$ $S_{A4}$'). If one switch of the pair is switched ON, the other complementary switch of same pair must be OFF. The switches are clamped by DC-link together with flying capacitors. The four switches ($S_{A1}$ to $S_{A4}$) must be connected in series between DC input and load and likewise for ($S_{A1}$'to $S_{A4}$'). The three flying capacitors $C_{A1}$, $C_{A2}$ and $C_{A3}$ are charged to different voltage levels. By changing the transistor switching states, the capacitors and the DC source are connected in different ways to produce various load voltages. Typical switch combinations for obtaining different output voltage levels are shown in Table 1 where '+' denotes charging and '–' denotes discharging of capacitors while NC indicates neither charging nor discharging. Chosen FCMLI is simulated using MATLAB-SIMULINK.

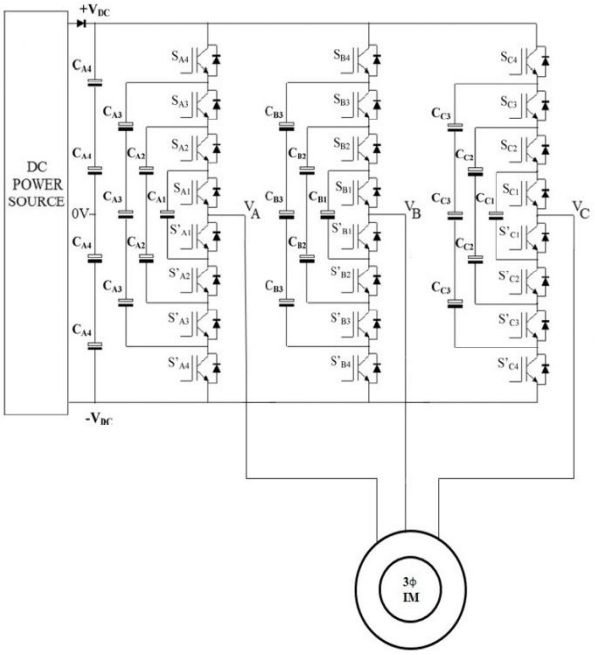


**Figure 1: A three phase five level FCMLI**

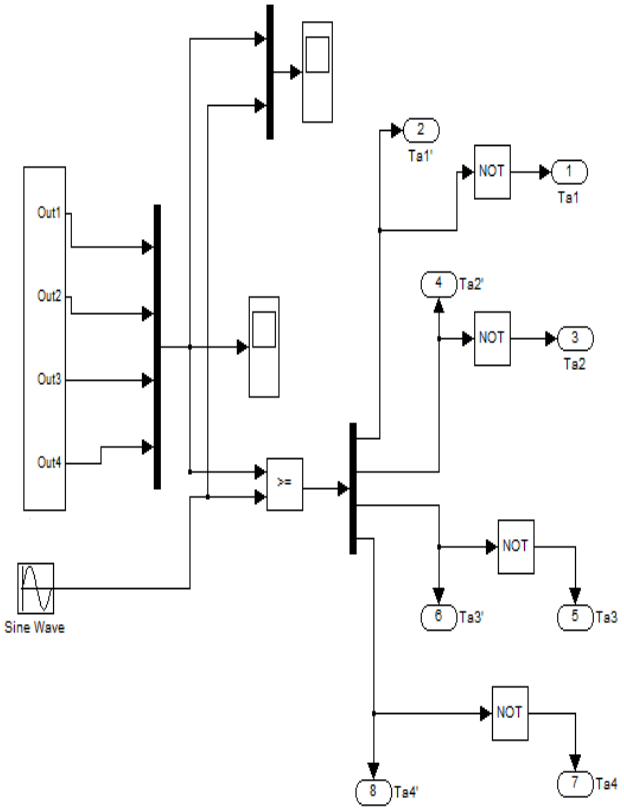


**Figure 2: Sample PWM generation logic developed for PDPWM technique using SIMULINK**

The steps to synthesis the five level phase a output voltage in this work are as follows:

a. For phase a output voltage of $V_{AN}$=0, two upper switches $S_{A3}$, $S_{A4}$ and two lower switches $S_{A1}$' and $S_{A2}$' are turned on.

b. For an output voltage of $V_{AN}=V_{dc}/4$, three upper switches $S_{A1}$, $S_{A2}$, $S_{A3}$ and one lower switch $S_{A4}$' are turned on.

c. For an output voltage of $V_{AN}=V_{dc}/2$, all upper switches $S_{A1}$ through $S_{A4}$ are turned on.

d. To obtain the output voltage of $V_{AN}= -V_{dc}/4$, upper switch $S_{A1}$ and three lower switches $S_{A2}$', $S_{A3}$' and $S_{A4}$' are turned on.

e. For an output voltage of $V_{AN} = -V_{dc}/2$, all lower switches $S_{A1}$' through $S_{A4}$' are turned on.

The phase a output voltage $V_{AN}$ has five states: Vdc/2, Vdc/4, 0, - Vdc/4 and - Vdc/2. The gate signals for the chosen five level FCMLI are developed using MATLAB-SIMULINK. The gate signal generator model developed is tested for various values of modulation index. The results of the simulation study are presented in this work in the form of the PWM outputs of the chosen multilevel inverter.

**Table 1: Switching scheme for one phase of three phase five level FCMLI**

| $S_{A1}$ | $S_{A2}$ | $S_{A3}$ | $S_{A4}$ | $C_{A3}$ | $C_{A4}$ | $C_{A5}$ | $V_{AN}$ |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | NC | NC | NC | $+V_{dc}/2$ |
| 1 | 1 | 1 | 0 | NC | NC | + | $+V_{dc}/4$ |
| 1 | 1 | 0 | 1 | NC | + | - | |
| 1 | 0 | 1 | 1 | + | - | NC | |
| 0 | 1 | 1 | 1 | - | NC | NC | |
| 0 | 0 | 1 | 1 | NC | - | NC | 0 |
| 0 | 1 | 0 | 1 | - | + | - | |
| 0 | 1 | 1 | 0 | - | NC | + | |
| 1 | 0 | 0 | 1 | + | NC | - | |
| 1 | 0 | 1 | 0 | + | - | + | |
| 1 | 1 | 0 | 0 | NC | + | NC | |
| 1 | 0 | 0 | 0 | + | NC | NC | $-V_{dc}/4$ |
| 0 | 1 | 0 | 0 | - | + | NC | |
| 0 | 0 | 1 | 0 | NC | - | + | |
| 0 | 0 | 0 | 1 | NC | NC | - | |
| 0 | 0 | 0 | 0 | NC | NC | NC | $-V_{dc}/2$ |

## 3. MULTI CARRIER BASED PWM METHODS

This work used the intersection of a sine wave with a triangular wave to generate firing pulses for a five level inverter. There are many alternative strategies to implement this. They are as given below.

a. Phase disposition PWM strategy.

b. Phase opposition disposition PWM strategy.

c. Alternate phase opposition disposition PWM strategy.

d. Carrier overlapping PWM strategy.

e. Variable frequency PWM strategy.

f. Phase shift PWM strategy.

### 3.1 Phase Disposition PWM Strategy

The rules for phase disposition method (Fig.3) for chosen five level inverter are

a. 4 carrier waveforms in phase are arranged.

b. The converter is switched to + Vdc/2 when the sine wave is greater than both upper carriers.

c. The converter is switched to + Vdc/4 when the sine wave is greater than first upper carrier.

d. The converter is switched to zero when sine wave is lower than upper carrier but higher than the lower carrier.

e. The converter is switched to – Vdc/4 when the sine wave is less than first lower carrier.

f. The converter is switched to - Vdc/2 when the sine wave is less than both lower carriers.

The following formula is applicable to sub harmonic PWM strategy i.e. PD, POD and APOD

The frequency modulation index

$$m_a = \frac{f_c}{f_m}$$

The amplitude modulation index

$$m_a = \frac{2A_m}{(m-1)A_c}$$

where
$f_c$ – Frequency of the carrier signal
$f_m$ – Frequency of the reference signal
$A_m$ –Amplitude of the reference signal
$A_c$ – Amplitude of the carrier signal
m – number of levels.

In this paper, $m_f$ = 40 and ma is varied from 0.6 to 1. $m_f$ is chosen as 40 as a trade off in view of the following reasons:

a. to reduce switching losses (which may be high at large $m_f$)

b. to reduce the size of the filter needed for the closed loop control, the filter size being moderate at moderate frequencies

c. to effectively utilise the available dSPACE system for hardware implementation.

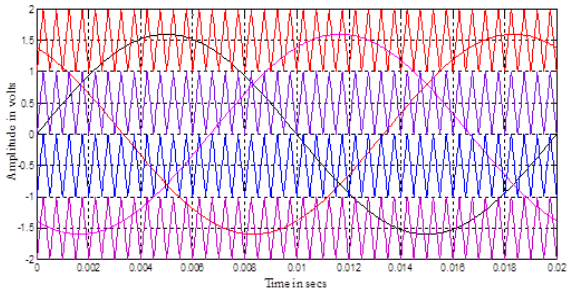


**Figure 3: Carrier arrangement for PDPWM strategy ($m_a$=0.8 and $m_f$=40)**

## 3.2 Phase Opposition Disposition Strategy

Four carrier waveforms are arranged so that all carrier waveforms above zero are in phase and they are 180 degrees out of phase with those below zero (Fig.4)

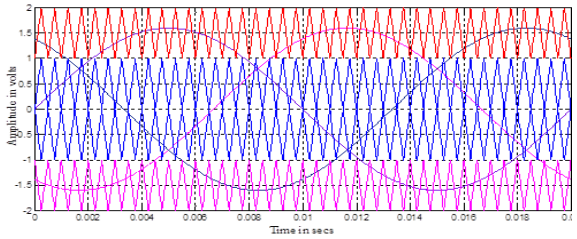


**Figure 4: Carrier arrangement for PODPWM strategy ($m_a$=0.8 and $m_f$=40)**

## 3.3 Alternative Phase Opposition and Disposition (APOD) Strategy

Carriers are arranged in such a manner that each carrier is out of phase with its neighbor by 180 degrees (Fig.5).

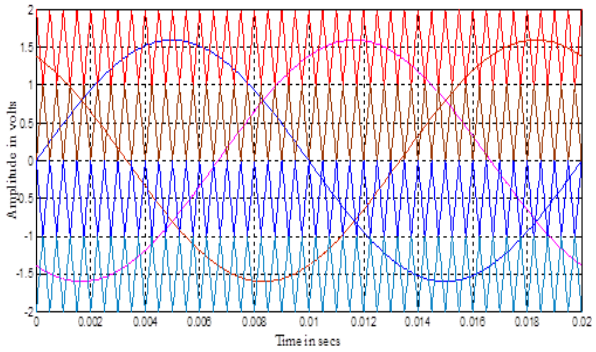


**Figure 5: Carrier arrangement for APODPWM strategy ($m_a$=0.8 and $m_f$=40)**

## 3.4 Phase Shift PWM (PSPWM) Strategy

The phase shift multicarrier PWM technique (Fig.6) uses four carrier signals of the same amplitude and frequency which are shifted by 90 degrees to one another to generate the five level inverter output voltage. The gate signals for the chosen inverter can be derived directly from the PWM signals (comparison of the carrier with the sinusoidal reference).

$$m_a = \frac{A_m}{A_c/2}$$

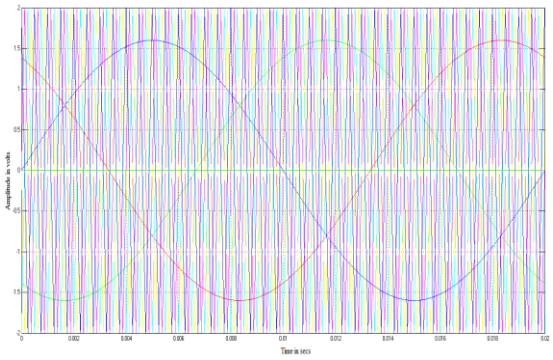

**Figure 8: Carrier arrangement for VFPWM strategy ($m_a$=0.8 , $m_f$=40(Upper and Lower Switches) and $m_f$=80(Intermediate Switches))**

## 4. SIMULATION RESULTS

The three phase flying capacitor five level inverter is modeled in SIMULINK using power system block set. Simulations are performed for different values of $m_a$ ranging from 0.6 to 1 and the corresponding %THD are measured using the FFT block and their values are shown in Table 2. Figs. 9 – 26 show the simulated output voltages of FCMLI fed IM and their harmonic spectra, speed and torque characteristics of Induction Motor (IM) with above strategies but for only one sample value of $m_a$ = 0.8. Fig. 10 shows the five level output voltage

generated by PDPWM strategy and its FFT plot is shown in Fig. 11. From Fig. 11, it is observed that the PDPWM strategy produces significant 30th, 32nd, 37th and 39th harmonic energy. Fig 13 shows the five level output voltage generated by PODPWM strategy and its FFT plot is shown in Fig. 14. From Fig. 14, it is observed that the PODPWM strategy produces significant 33rd and 35th harmonic energy. Fig 16 shows the five level output voltage generated by APODPWM strategy and its FFT plot is shown in Fig. 17. From Fig. 17, it is observed that the APODPWM strategy produces significant 35th and 37th harmonic energy. Fig 19 shows the five level output voltage generated by COPWM strategy and its FFT plot is shown in Fig. 20. From Fig. 20, it is observed that the COPWM strategy produces significant 3rd, 4th, 5th, 6th, 34th, 35th, 36th, 37th and 38th harmonic energy. Fig 22 shows the five level output voltage generated by VFPWM strategy and its FFT plot is shown in Fig. 23. From Fig. 23, it is observed that the VFPWM strategy produces significant 34th and 38th harmonic energy. Fig 25 shows the five level output voltage generated by PSPWM strategy and its FFT plot is shown in Fig. 26. From Fig. 26, it is observed that the PSPWM strategy produces no significant harmonic energy. Figs. 9, 12, 15, 18, 21, 24 show speed torque characteristics of chosen MLI fed IM for various PWM strategies. The following parameter values are used for simulation : $V_{dc}$ = 440V , induction motor load – 50HP(37 KW), 400V, 50Hz, 1480rpm, $T_m$ = 4Nm, $f_c$ = 2000Hz, $f_m$ = 50Hz.

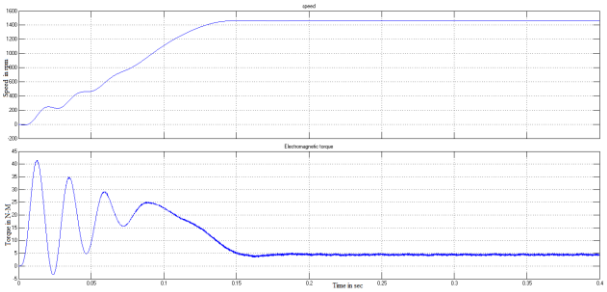

**Figure 9: Speed and torque characteristics of IM for PDPWM strategy**

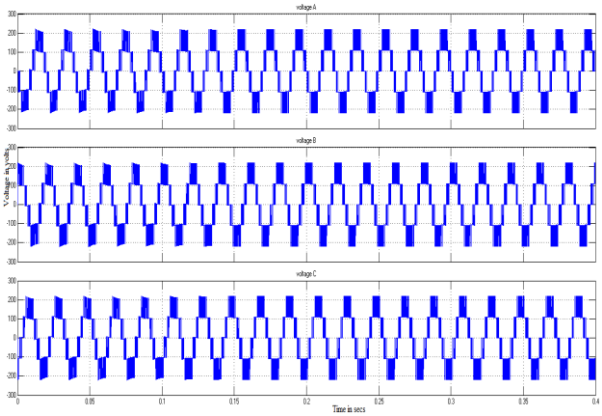

**Figure 10: Output voltage generated by PDPWM strategy for IM load**

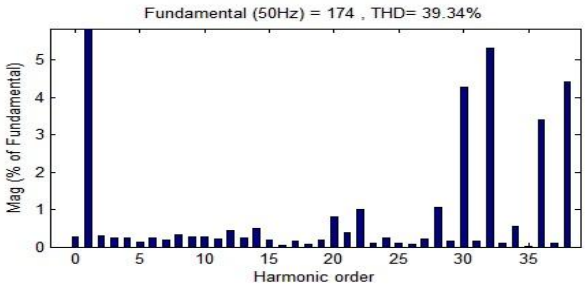


**Figure 11: FFT plot for output voltage of PDPWM strategy for IM load**

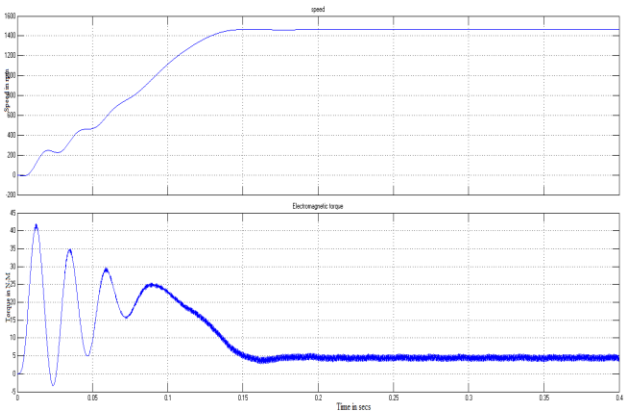

**Figure 12: Speed and torque characteristics of IM for PODPWM strategy**

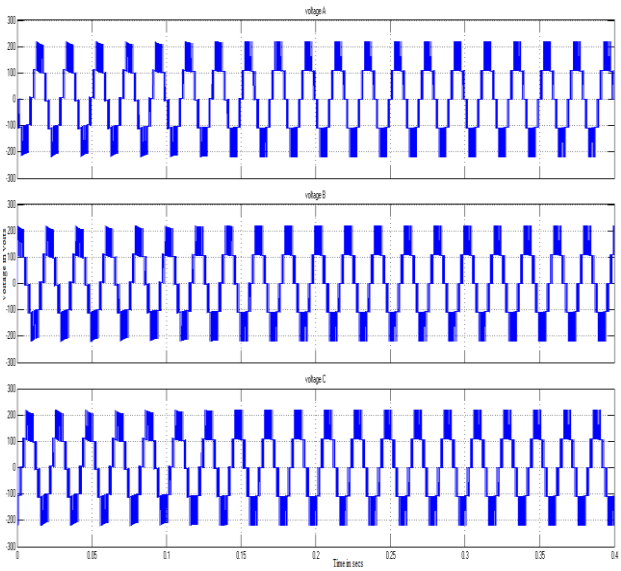

**Figure 13: Output voltage generated by PODPWM strategy for IM load**

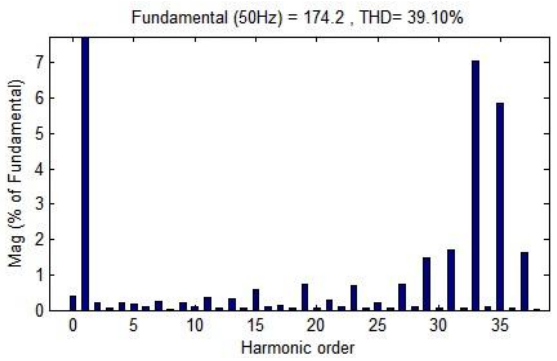


**Figure 14: FFT plot for output voltage of PODPWM strategy for IM load**

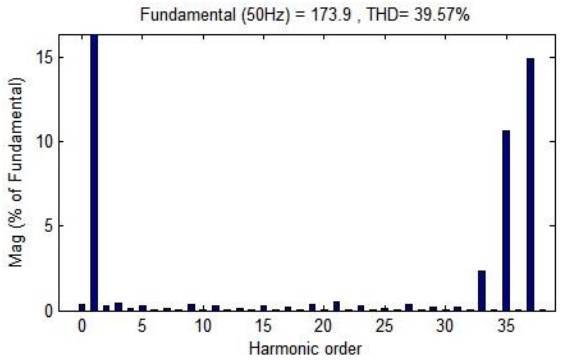


**Figure 17: FFT plot for output voltage of APODPWM strategy for IM load**

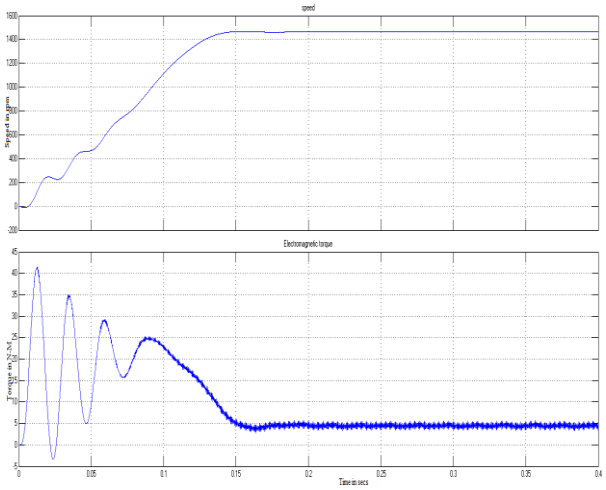

**Figure 15: Speed and torque characteristics of IM for APODPWM strategy**

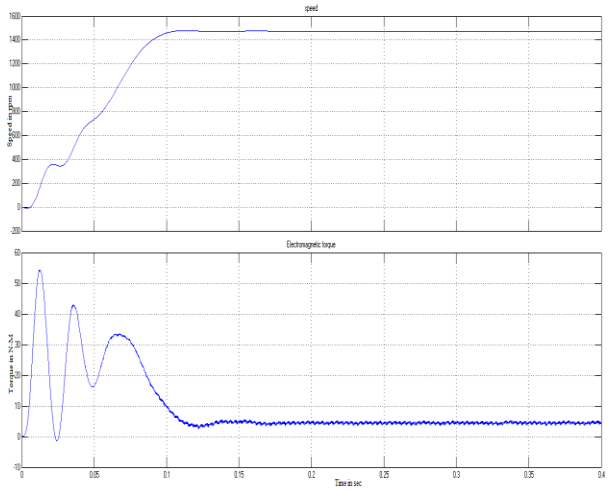

**Figure 18: Speed and torque characteristics of IM for COPWM strategy**

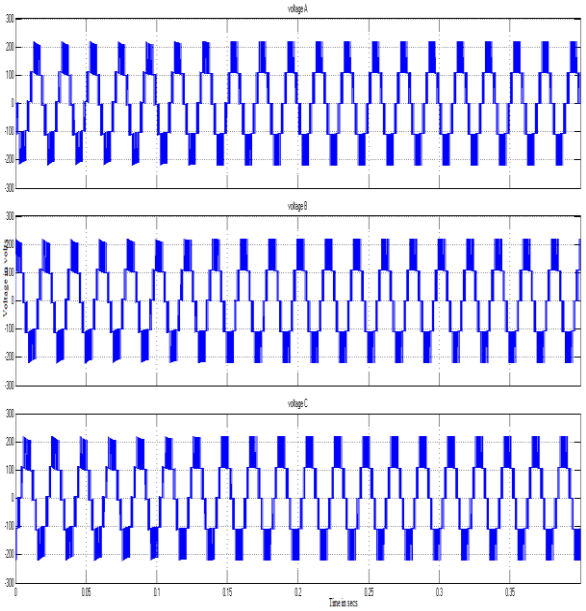

**Figure 16: Output voltage generated by APODPWM strategy for IM load**

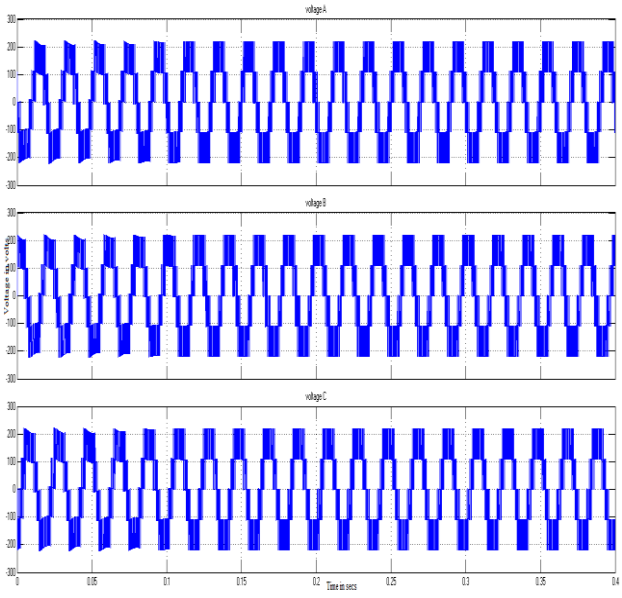

**Figure 19: Output voltage generated by COPWM strategy for IM load**

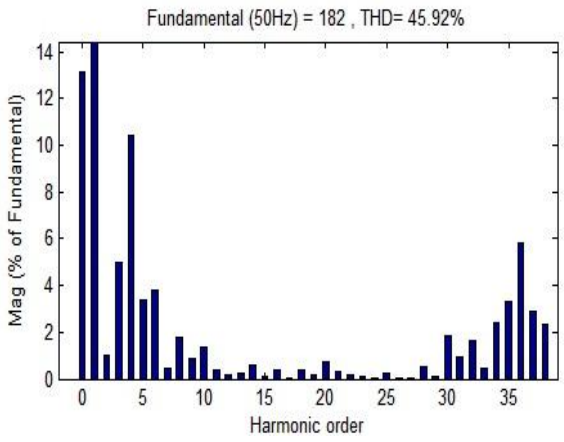


**Figure 20: FFT plot for output voltage of COPWM strategy for IM load**

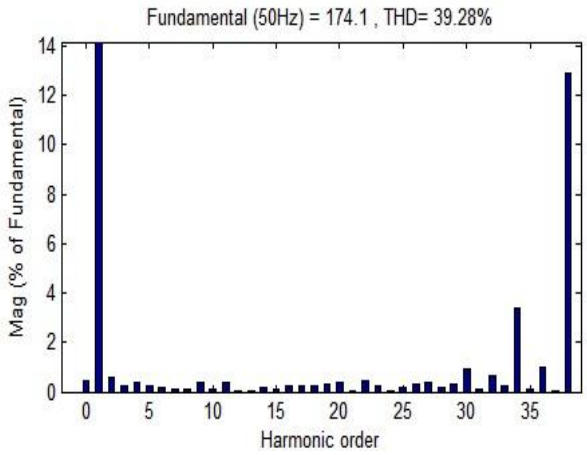


**Figure 23: FFT plot for output voltage of VFPWM strategy for IM load**

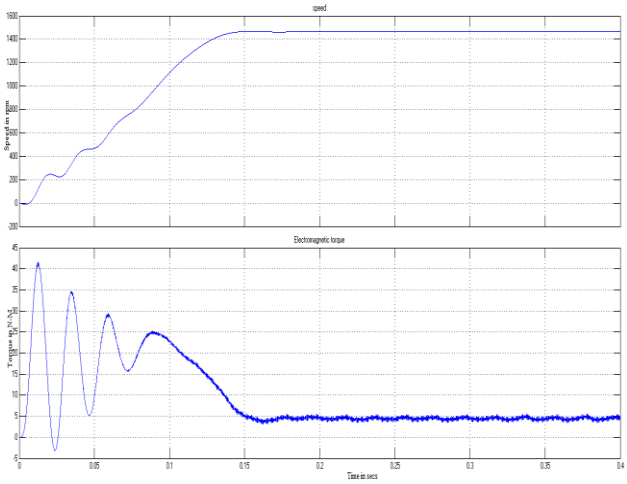

**Figure 21: Speed and torque characteristics of IM for VFPWM strategy**

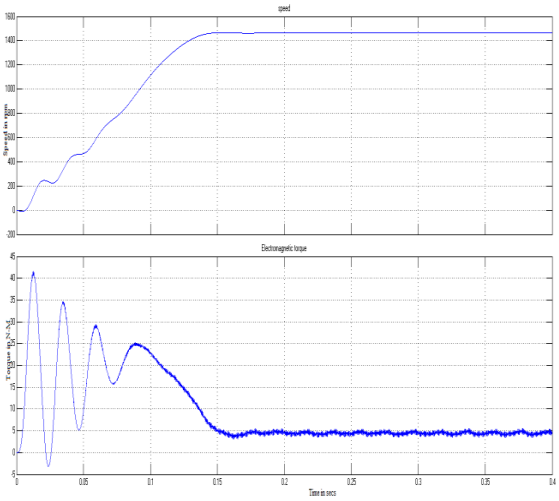

**Figure 24: Speed and torque characteristics of IM for PSPWM strategy**

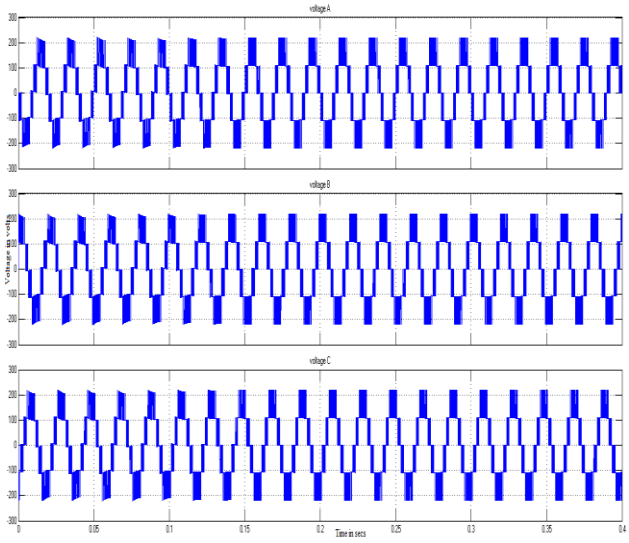

**Figure 22: Output voltage generated by VFPWM strategy for IM load**

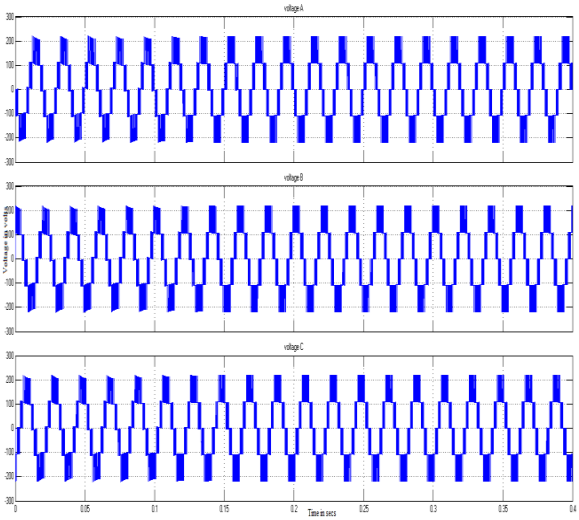

**Figure 25: Output voltage generated by PSPWM strategy for IM load**

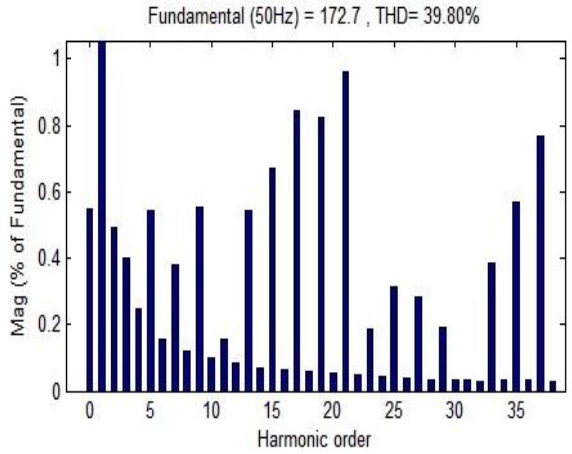


**Figure 26: FFT plot for output voltage of PSPWM strategy for IM load**

**Table 2: % THD comparison for different modulation indices for IM load**

| $m_a$ | PD | POD | APOD | CO | PS | VF |
|---|---|---|---|---|---|---|
| 1 | 27.63 | 27.32 | 28.13 | 32.65 | 28.14 | 27.66 |
| 0.9 | 34.44 | 34.31 | 34.85 | 39.18 | 34.09 | 34.29 |
| 0.8 | 39.34 | 39.10 | 39.57 | 45.92 | 39.8 | 39.28 |
| 0.7 | 43.08 | 42.93 | 43.16 | 55.7 | 43.02 | 43.5 |
| 0.6 | 45.39 | 45.32 | 45.32 | 66.8 | 45.95 | 45.44 |

**Table 3: VRMS (fundamental) for different modulation indices for IM load**

| $m_a$ | PD | POD | APOD | CO | PS | VF |
|---|---|---|---|---|---|---|
| 1 | 154.5 | 154.8 | 154.3 | 157.6 | 154.2 | 154.5 |
| 0.9 | 138.8 | 138.8 | 138.6 | 143.8 | 138.4 | 138.8 |
| 0.8 | 123 | 123.1 | 123 | 128.7 | 122.1 | 123.1 |
| 0.7 | 107.2 | 106.9 | 107.2 | 110.4 | 106.9 | 106.9 |
| 0.6 | 91.6 | 91.45 | 91.65 | 91.07 | 90.14 | 91.8 |

**Table 4: Crest factor for different modulation indices for IM load**

| $m_a$ | PD | POD | APOD | CO | VF |
|---|---|---|---|---|---|
| 1 | 1.414 | 1.4156 | 1.414 | 1.4144 | 1.4142 |
| 0.9 | 1.4139 | 1.4143 | 1.4145 | 1.414 | 1.4142 |
| 0.8 | 1.414 | 1.414 | 1.4142 | 1.414 | 1.4143 |
| 0.7 | 1.414 | 1.4137 | 1.414 | 1.414 | 1.414 |
| 0.6 | 1.4141 | 1.4146 | 1.4144 | 1.4139 | 1.414 |

**Table 5: Form factor for different modulation indices for IM load**

| $m_a$ | PD | POD | APOD | CO | VF |
|---|---|---|---|---|---|
| 1 | 120.74 | 125.04 | 121.83 | 126.2 | 137.83 |
| 0.9 | 104.6 | 112.39 | 110.58 | 135.64 | 112.47 |
| 0.8 | 111.61 | 107.79 | 104.6 | 119.12 | 102.89 |
| 0.7 | 77.14 | 101.48 | 96.88 | 113.2 | 83.93 |
| 0.6 | 74.01 | 81.19 | 84.67 | 97.87 | 80.27 |

## 5. CONCLUSION

In this work the simulation results of three phase five level flying capacitor multilevel inverter fed induction motor load with various modulating strategies are obtained through MATLAB/SIMULINK. The output quantities like phase voltage, THD spectrum for phase voltage, and torque-speed characteristics of induction motor are obtained. It is observed from Table 2 that PODPWM method provides output with relatively low distortion. COPWM is also found to perform better (Table 3) since it provides relatively higher fundamental RMS output voltage. Table 4 and 5 show the crest factor and form factor.

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