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A Novel Reversible Gate and its Applications

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ABSTRACT

The development of computing machines found great success in the last decades. But the ongoing miniaturization of integrated circuits will reach its limits in the near future. Shrinking transistor sizes and power dissipation are the major constraints in the development of smaller and more complex circuits. Reversible logic provides an alternative that may overcome many of these problems in the future. For low-power design, reversible logic gates are very much in demand for the future computing technologies as they are known to produce zero power dissipation under ideal conditions. This paper proposes design of new reversible logic gate and some of its applications. The quantum cost of a reversible logic circuit can be minimized by reducing the number of reversible logic gates.

Keywords: *Reversible logic circuits, Quantum computing, Nanotechnology, Multiplexer.*

1. INTRODUCTION

Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. Quantum computers are constructed using reversible logic circuits. It has wide applications in low power CMOS and Optical information processing, DNA computing, quantum computation and nanotechnology. In 1960 R.Landauer demonstrated that high technology circuits and systems constructed using irreversible hardware result in energy dissipation due to information loss [1]. According to Landauer's principle, the loss of one bit of information dissipates KTln2 joules of energy where K is the Boltzmann's constant and T is the absolute temperature at which the operation is performed [1]. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components. In 1973, Bennett, showed that one can avoid KTln2 joules of energy dissipation constructing circuits using reversible logic gates [2].

This paper is organized as follows: Section II gives the brief introduction of the reversible logic gates. Section III describes the design of new reversible gate and its applications using existing reversible gates and proposed gate. Section IV gives the results and discussions of the proposed design. Finally Section V concludes with a scope for further research.

2. REVERSIBLE LOGIC GATES

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-out is not allowed as one–to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits [3, 4 and 12].

- The number of Reversible gates (N): The number of reversible gates used in circuit.
- The number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.
- Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive

reversible logic gates (1*1 or 2*2) required to realize the circuit.

- Gate levels (GL): This refers to the number of levels in the circuit which are required to realize the given logic functions [12].

2.1 Basic Reversible Logic Gates

2.1.1 Feynman Gate

Fig.1 shows a 2*2 Feynman gate [6]. The input vector is I (A, B) and the output vector is O (P, Q). The outputs are defined by P=A, Q=A⊕B. Quantum cost of a Feynman gate is 1.

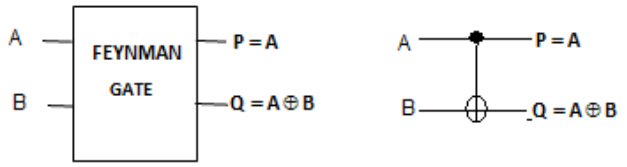

Fig 1: Feynman gate

2.1.2 Double Feynman Gate (F2G)

Fig.2 shows a 3*3 Double Feynman gate [7]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P = A, Q=A⊕B, R=A⊕C. Quantum cost of double Feynman gate is 2.

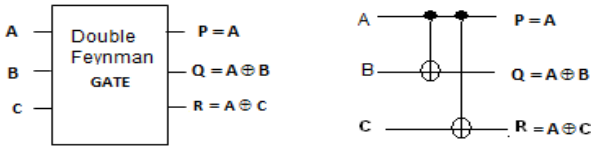

Fig 2: Double Feynman gate

2.1.3 Toffoli Gate

Fig 3 shows a 3*3 Toffoli gate [3]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P=A, Q=B, R=AB⊕C. Quantum cost of a Toffoli gate is 5.

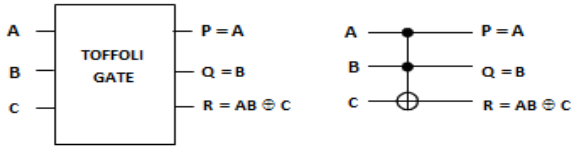

Fig 3: Toffoli gate

2.1.4 Fredkin Gate

Fig 4 shows a 3*3 Fredkin gate [4]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B⊕AC and R=A′C⊕AB. Quantum cost of a Fredkin gate is 5.

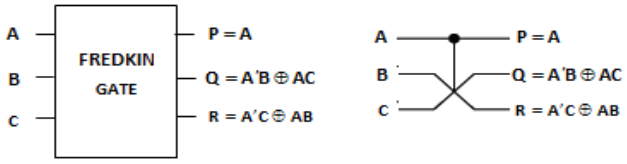

Fig 4: 3*3 Fredkin gate

2.1.5 Peres Gate

Fig 5 shows a 3*3 Peres gate [10]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A⊕B and R=AB⊕C. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.

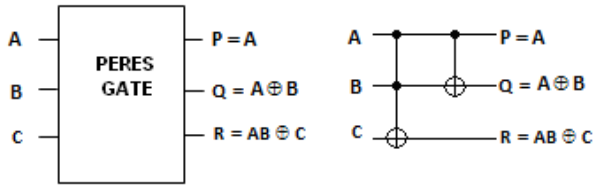

Fig 5: Peres gate

3. PROPOSED GATE

FIG 6 shows the proposed gate, SSG. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P=A, Q=A B + A C, R= A C + A B .The truth table is shown in table1. The quantum cost of the proposed gate is 4.

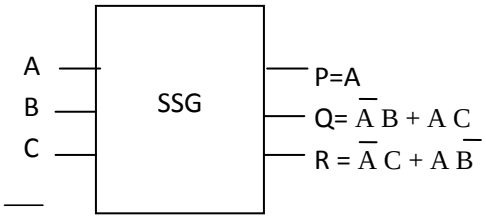

Fig 6: proposed gate, SSG

Table 1: Truth table of SSG

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1

1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	1	0	0
1	1	1	1	1	0

The SSG can be used for many applications. Some of the applications are explained here.

3.1 Applications

The proposed gate, SSG can be used as half adder, half subtractor, full adder and full subtractor.

3.1.1 Half Adder

The half adder and its truth table is shown in fig 7 and table2. The Half adder using proposed and Feynman gate is shown in fig 8 and 9.

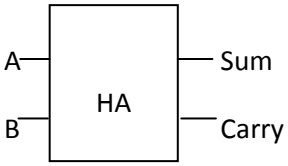

Fig 7: half adder

Table 2: Half adder truth table

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

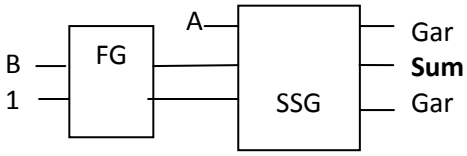

Fig 8: Sum of Half Adder

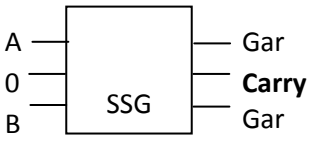

Fig 9: Carry of Half Adder

3.1.2 Half Subtractor

The half subtractor and its truth table is shown in fig 10 and table3. The half subtractor using proposed and Feynman gate is shown in fig 11 and 12.

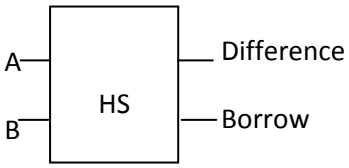

Fig 10: half subtractor

Table 3: Half subtractor truth table

A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

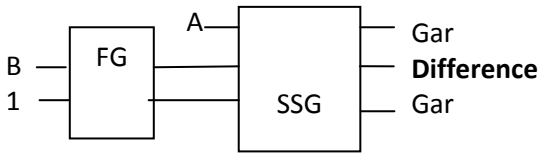

Fig 11: Difference of Half Subtractor

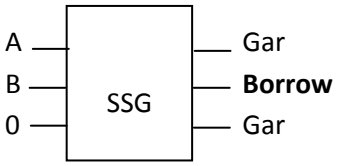

Fig 12: Borrow of Half Subtractor

3.1.3 Full Adder

The full adder and its truth table is shown in fig 13 and table4. The full adder using proposed and Feynman gate is shown in fig 14.

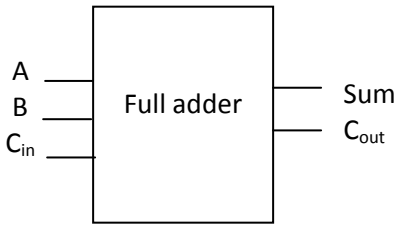

Fig13: Full adder

Table 4: Full adder truth table

A	B	C	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

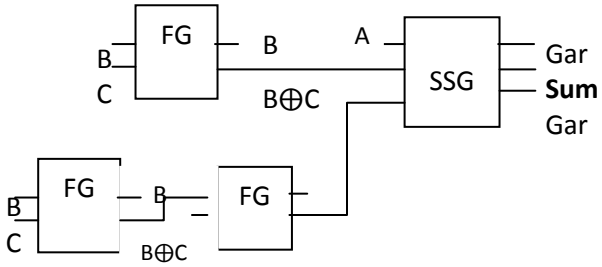

Fig 14: Sum of full adder

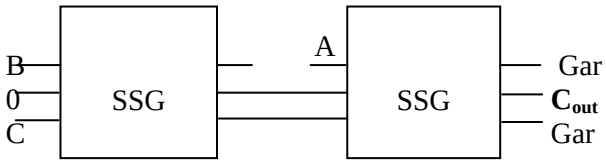

Fig 15: Carry of Full adder

3.1.4 Full Subtractor

The full subtractor and its truth table is shown in fig 16 and table 5. The full adder using proposed and Feynman gate is shown in fig 17and 18.

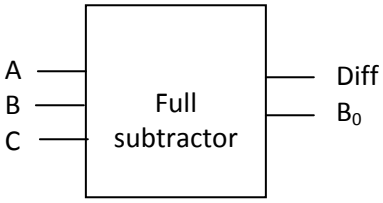

Fig16: Full subtractor

Table 5: Full subtractor truth table

A	B	C	D	B_0
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

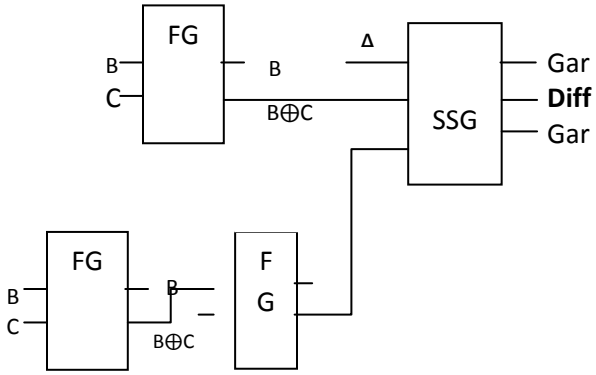

Fig 17: Difference of full subtractor

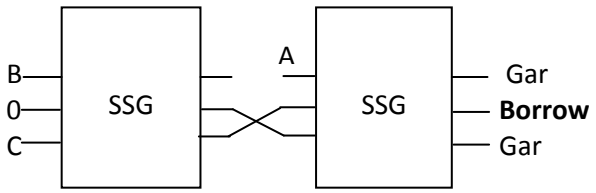

Fig 18: Borrow of Full subtractor

4. SIMULATION RESULTS

The behavior of the proposed gate, SSG and arithmetic circuits such as half adder, half subtractor , full adder and full subtractor using SSG are verified using Xilinx ISE and simulated using ModelSim. The simulated results are shown in figs 19-23.

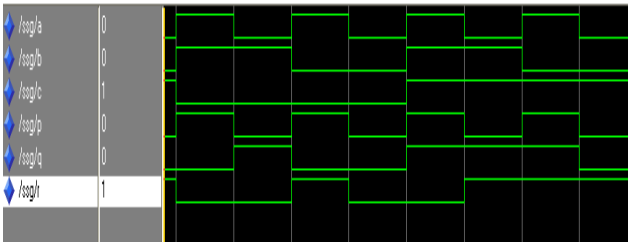

Fig 19: Simulation result of SSG

Fig 20: Simulation result of half adder

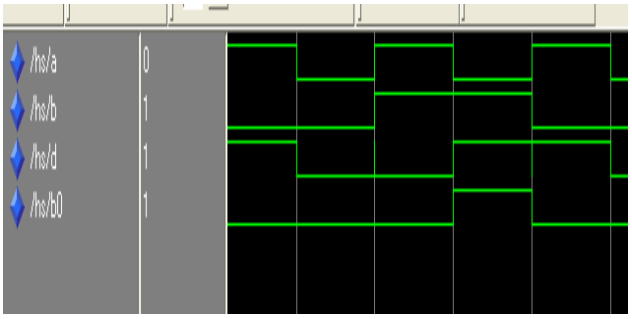

Fig 21: Simulation result of half subtractor

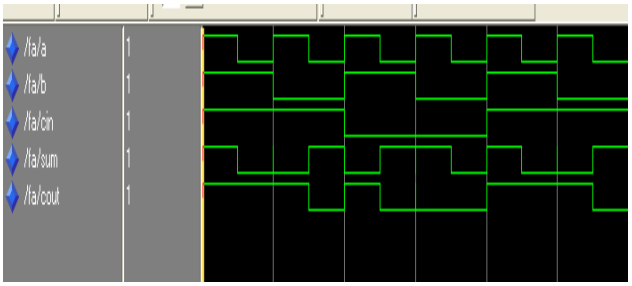

Fig 22: Simulation result of full adder

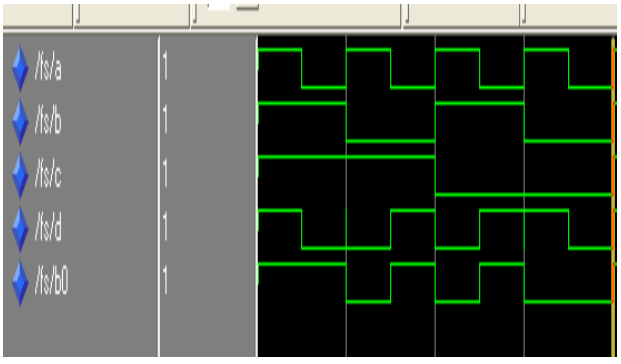

Fig 23: Simulation result of full subtractor

5. CONCLUSION

In this paper, we presented a new gate SSG, and its applications such as half adder, half subtractor, full adder and full subtractor. The adders and subtractors were designed using Feynman gate and SSG. The proposed gate can be used for many complex arithmetic circuits. The proposed circuit has less number of garbage outputs. These circuits are used in low power applications such as Quantum computers and Nanotechnology.

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