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Design of Universal Shift Register Using Reversible Logic

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ABSTRACT

Reversible sequential circuits are considered the significant memory block for their ultra-low power consumption. Universal shift register is an important memory element of the sequential circuit family. In this paper we proposed efficient design of reversible universal shift register that is optimized in terms of quantum cost, delay and garbage outputs. Appropriate theorems and lemmas are presented to clarify the proposed designs and establish its efficiency.

Keywords: *Flip-Flop, Garbage Output, Multiplexer, Reversible Logic, Reversible Gate, Shift Register, Quantum Cost.*

1. INTRODUCTION

In recent year reversible logic has been considered as an important issue for computer design. The primary reason for this is the increasing demands for lower power devices. It has been demonstrated by Landauer [1] that circuits and systems constructed using irreversible logic will result in power consumption and energy dissipation due to information loss and the loss of one bit of information dissipates kT*ln2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. Bennett [2] showed that to avoid the heat dissipation, circuits must be built using reversible logic gates only.

Reversible computing does not result in information loss during the computation process. Thus, it naturally takes care of heating generated due to information loss. Despite the great potential of reversible logic and these endorsements from the leaders in the field, little work has been done in the area of sequential reversible logic. We studied the existing work in this area and proposed a new efficient design for universal shift register. For this we modified the existing Frekdin gate (FRG) in two ways and named Modified FRG1 to design efficient 4-to-1 multiplexer and Modified FRG2 to design D flip-flop.

The main challenges of designing reversible circuits are to reduce the number of gates, garbage outputs, constant inputs, propagation delay and quantum cost. While designing the proposed universal shift register, we optimized the quantum cost, the number of garbage outputs and delay of the proposed design.

This paper consists of the following sections: Section 2 describes some basic definitions related to reversible logic, Section 3 describes some popular reversible logic gates and their quantum representations, Section 4 describes our proposed modification on Frekdin gate (FRG), Section 5 presented the logic synthesis and design of our proposed Universal Shift Register, Section 6 compares our design with the existing designs available in literature and finally this paper is concluded with Section 7.

2. BASIC DEFINITIONS

In this section, some basic definitions related to reversible logic are presented. We formally define reversible gate, garbage output, delay in reversible circuit and quantum cost of reversible gate.

2.1 Reversible Gate

A Reversible Gate is a k-input, k-output (denoted by k*k) circuit that produces a unique output pattern for each possible input pattern [3]. Reversible Gates are circuits in which the number of outputs and inputs are equal and there is a one to one mapping between the vector of inputs and outputs. If the input vector is Iv where $Iv = (I_{1,j}, I_{2,j}, I_{3,j}, \ldots, I_{k-1,j}, I_{k,j})$ and the output vector is Ov where $Ov = (O_{1,j}, O_{2,j}, O_{3,j}, \ldots, O_{k-1,j}, O_{k,j})$, then according to the definition, for each particular vector j, Iv « Ov.

2.2 Garbage Output

Unwanted or unused outputs which are needed to maintain reversibility of a reversible gate (or circuit) are known as Garbage Outputs. The garbage output of Feynman gate [4] is shown Figure 1 with *.

2.3 Delay

The delay of a logic circuit is the maximum number of gates in a path from any input line to any output line. This definition is based on the assumptions that: (i) Each gate performs computation in one unit time and (ii) All inputs to the circuit are available before the computation begins.

In this paper, we use the logical depth as measure of the delay proposed by Mohammadi and Eshghi [5]. The delay of each 1x1 gate and 2×2 reversible gate is taken as unit delay 1. Any 3×3 reversible gate can be designed from 1×1 reversible gates and 2×2 reversible gates, such as CNOT gate, Controlled-V and Controlled-V^+ gates (V is a square-root-of NOT gate and V^+ is its hermitian). Thus, the delay of a 3×3 reversible gate can be computed by calculating its logical depth when it is designed from smaller 1×1 and 2×2 reversible gates.

2.4 Quantum Cost

The quantum cost of a reversible gate is the number of 1×1 and 2×2 reversible gates or quantum logic gates required in its design. The quantum costs of all reversible 1×1 and 2×2 gates are taken as unity [6]. In simple terms, the quantum cost of a reversible gate can be calculated by counting the numbers of NOT, Controlled-V, Controlled-V^+ and CNOT gates required in its implementation.

3. QUANTUM ANALYSIS OF DIFFERENT REVERSIBLE GATES

Every reversible gate can be calculated in terms of quantum cost and hence the reversible circuits can be measured in terms of quantum cost. Reducing the quantum cost from reversible circuit is always a challenging one and works are still going on in this area. This section describes some popular reversible gates and quantum equivalent diagram of each reversible.

3.1 Feynman Gate

The input vector, I_v and output vector, O_v for 2*2 Feynman Gate (FG) is defined as follows: $I_v = (A, B)$ and $O_v = (P = A, Q = A \oplus B)$. The quantum cost of Feynman gate is 1. The block diagram and equivalent quantum representation for 2*2 Feynman gate are shown in Fig 1.

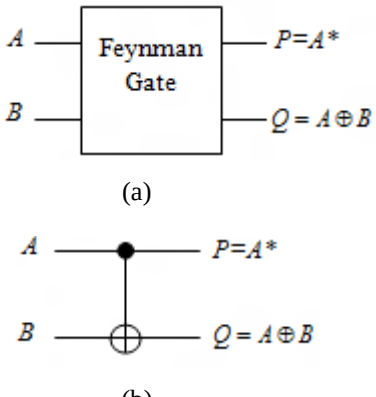

Figure 1. (a) Block diagram of 2x2 Feynman gate and (b) Equivalent quantum representation

3.2 Toffoli Gate

The input vector, I_v and output vector, O_v for 3*3 Toffoli gate (TG) [7] is defined as follows: $I_v = (A, B, C)$ and $O_v = (P = A, Q = B, R = AB \oplus C)$. The quantum cost of Toffoli gate is 5. The block diagram and equivalent quantum representation for 3*3 Toffoli gate are shown in Figure 2.

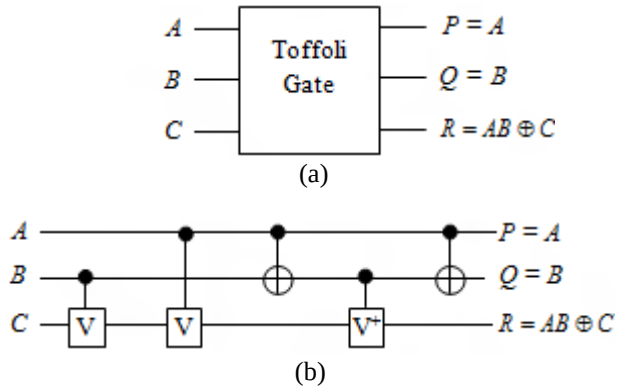

Figure 2. (a) Block diagram of 3*3 Toffoli gate and (b) Equivalent quantum representation.

3.3 Fredkin Gate

The input vector, I_v and output vector, O_v for 3*3 Fredkin gate (FRG) [8] is defined as follows: $I_v = (A, B, C)$ and $O_v = (P=A, Q = \bar{A}B \oplus AC, R = \bar{A}C \oplus AB)$. The quantum cost of Frekdin gate is 5. The block diagram and equivalent quantum representation for 3*3 Fredkin gate are shown in Figure 3.

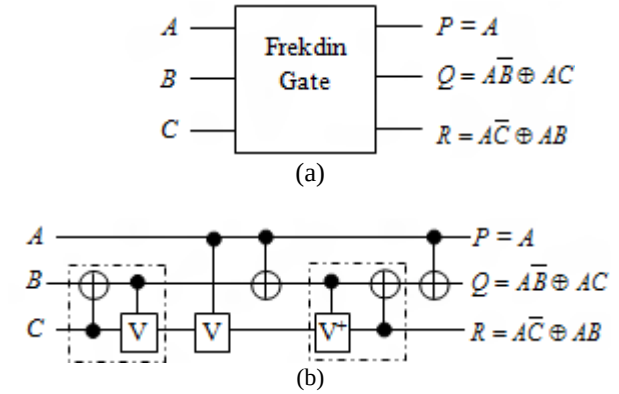

Figure 3. (a) Block diagram of 3*3 Frekdin gate and (b) Equivalent quantum representation

3.4 Peres Gate

The input vector, I_v and output vector, O_v for 3*3 Peres gate (PG)[9] is defined as follows: $I_v = (A, B, C)$ and $O_v = (P = A, Q = A \oplus B, R = AB \oplus C)$. The quantum cost of Peres gate is 4. The block diagram and equivalent quantum representation for 3*3 Peres gate are shown in Figure 4.

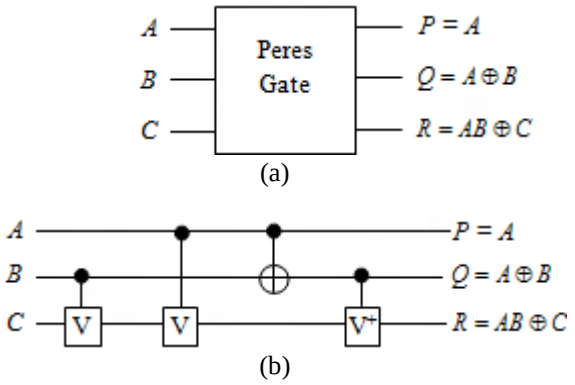

Figure 4. (a) Block diagram of 3*3 Peres and (b) Equivalent quantum representation.

4. PROPOSED MODIFIED FREKDIN GATE

4.1 Modified FRG 1 Gate

The input vector, I_v and output vector, O_v for 3*3 modified Fredkin Gate (Modified FRG 1) is defined as follows: I_v = *(A, B, C)* and O_v = ($P=A$, $Q = A \oplus \bar{A}B \oplus AC = \bar{A}B \oplus A\bar{C}$, $R = \bar{A}C \oplus AB$). The quantum cost of Modified FRG1 gate is 4.

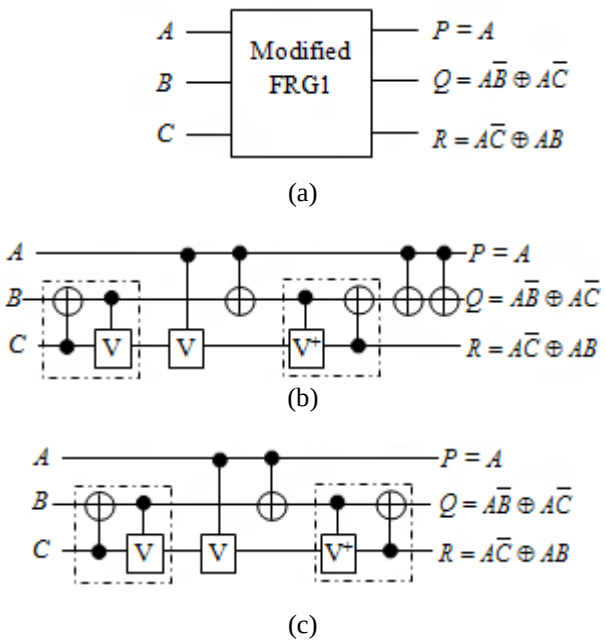

Figure 5. (a) Block diagram of Modified FRG1, (b) and (c) Equivalent quantum representation

4.2 Modified FRG 2 Gate

The input vector, I_v and output vector, O_v for 3*3 modified Fredkin Gate (Modified FRG 2) is defined as follows: I_v = *(A, B, C)* and O_v = ($P=\bar{A}$, $Q = \bar{A}B \oplus A\bar{C}$, $R = \bar{A}C \oplus AB$). The quantum cost of Modified FRG2 gate is 5.

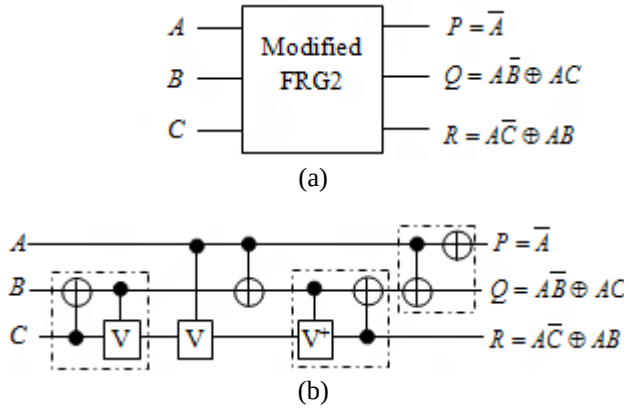

Figure 6. (a) Block diagram of Modified FRG2 gate and (b) Equivalent quantum representation

5. DESIGN OF REVERSIBLE UNIVERSAL SHIFT REGISTER

In this section we presented novel designs of reversible universal shift register and its components that are optimized in terms of quantum cost, delay and garbage outputs.

5.1 Proposed Universal Shift Register

Universal shift registers store binary data and can be shifted left or right when a clock signal is applied. All modes of operation such as serial-in serial-out (SISO), serial-in parallel-out (SIPO), parallel-in serial-out (PISO), parallel-in parallel-out (PIPO) can also be performed upon the occurrence of clock. Figure 7 shows our proposed universal shift register consists of 4 D flip-flop blocks and four 4-to-1 multiplexers.

The four multiplexers have two common selection inputs S_1 and S_0. Input 0 in each multiplexer is selected when S_1S_0 = 00, input 1 is selected when S_1S_0 =01, and similarly for other two inputs. The functional characteristic of the register is given in Table 1.

Table 1. Operations of Universal Shift Register

Mode Control		Register Operation
S_1	S_0	
0	0	No change
0	1	Shift Right
1	0	Shift Left
1	1	Parallel Load

When S_1S_0 = 00, the present value of the register is applied to the D inputs of the flip-flops. This condition forms a path from the output of each flip-flop into the input of the same flip-flop, so that the output recirculates to the input in this mode of operation. When S_1S_0 = 01 terminal 1 of the multiplexer inputs has a path to the D

inputs to the flip-flops. This causes right shift operation with the serial input transferred into flip-flop O_3. When S_1S_0 = 01 shift left operation results with other serial input going into the flip-flop O_0. Finally when S_1S_0 = 11, binary information in parallel input lines is transferred into register simultaneously during next clock pulse.

5.2 Proposed 4-to-1 Reversible Multiplexer

The characteristic equation of a 4-to-1 multiplexer is $F = I_0\bar{S}_0\bar{S}_1 + I_1S_0\bar{S}_1 + I_2\bar{S}_0S_1 + I_3S_0S_1$ which can be simplified as $F = \bar{S}_1\left(\bar{S}_0I_2 \oplus S_0I_3\right) \oplus S_1\left(\bar{S}_0I_0 \oplus S_0I_1\right)$. It can be realized by 3 Modified FRG1. The proposed 4-to-1 reversible multiplexer is shown in Figure 8.

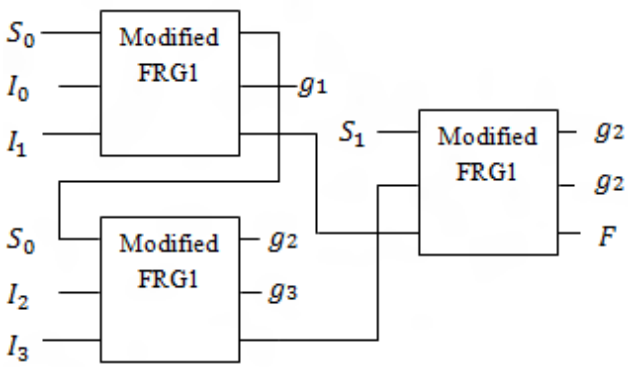

Figure 8. Proposed 4-to-1 Reversible Multiplexer

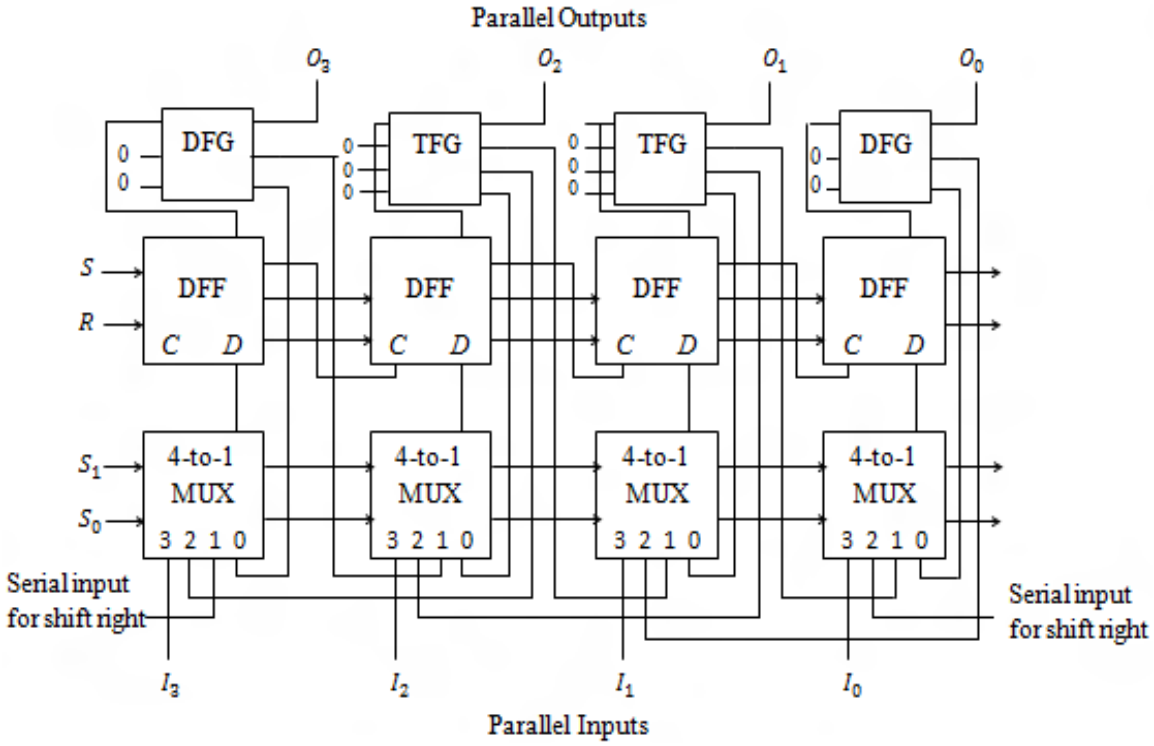

Figure 7. Proposed Reversible Universal Shift Register

5.3 Proposed D Flip-Flop

The characteristic equation of gated D flip-flop is $Q^+ = CLK.D+\overline{CLK}.Q$. The D flip-flop can be realized by one Modified FRG2 gate and one FG. It can be mapped with Modified FRG2 by giving CLK, D and Q respectively in 1st, 2nd and 3rd inputs of Modified FRG2 gate. The Figure 9 shows our proposed gated D flip-flop.

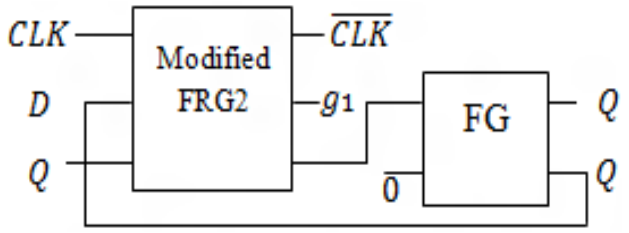

Figure 9. Proposed gated D flip-flop

For our shift register we need master slave D flip-flop with asynchronous inputs Set(S) and Reset(R). Our proposed Master Slave D flip-flop with asynchronous inputs is shown in Figure 10.

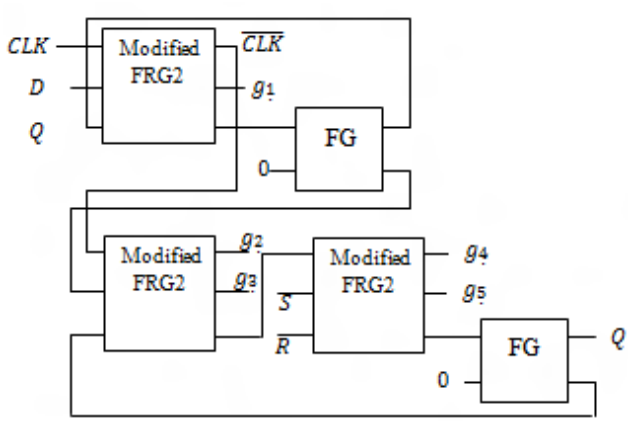

Figure 10. Proposed Master Slave D flip-flop with Asynchronous Inputs

6. RESULTS AND DISCUSSIONS

6.1 Evaluation of Proposed 4 – to - 1 Multiplexer

The proposed 4-to-1 Multiplexer has quantum cost 12, delay 12 and 5 garbage bits. The proposed design of 4-to-1 Multiplexer achieves improvement ratios of 20%, 20% and 0% in terms of quantum cost, delay and garbage outputs compared to the design presented in existing [10]. The results are summarized in Table 2.

Table 2. Comparison of 4-to-1 Multiplexer

Design of 4-to-1 Multiplexer	**Quantum Cost**	**Delay**	**Garbage Outputs**
Proposed	**12**	**12**	**5**
Existing[10]	15	15	5
Improvement (%)	20	20	0

6.2 Evaluation of Proposed Master Slave D Flip-flop with Asynchronous Inputs

The proposed Master Slave DFF with asynchronous inputs has quantum cost 14, delay 14 and 5 garbage bits. The proposed design of Master Slave DFF with asynchronous inputs achieves improvement ratios of 18%, 18% and 0% in terms of quantum cost, delay and garbage outputs compared to the design presented in existing [10]. The results are summarized in Table 3.

Table 3. Comparison of Master Slave DFF with Asynchronous Inputs

MSDFF (with asynchronous inputs)	**Quantum Cost**	**Delay**	**Garbage Outputs**
Proposed	**14**	**14**	**5**
Existing[10]	17	17	5
Improvement (%)	18	18	0

6.3 Evaluation of Proposed Reversible Universal Shift Register

The proposed Reversible Universal Shift Register has quantum cost 114, delay 114 and 40 garbage bits. The proposed design of Reversible Universal Shift Register achieves improvement ratios of 21%, 21% and 0% in terms of quantum cost, delay and garbage outputs compared to the design presented in existing [10]. The improvement ratios compared to the design presented in existing [11] and [12] are 5% and 5% in terms quantum cost and delay. The results are summarized in Table 4.

Table 4. Comparison of Reversible Universal Shift Register

Design of Universal Shift Register	**Quantum Cost**	**Delay**	**Garbage Outputs**
Proposed	114	114	40
Existing[10]	144	144	40
Existing[11]	120	120	36
Existing[12]	120	120	29
Improvement (%) w.r.t [10]	21	21	0
Improvement (%) w.r.t [11]	5	5	-
Improvement (%) w.r.t [12]	5	5	-

7. CONCLUSION

Universal shift register is an important sequential memory element. In this paper we proposed a novel approach of designing an optimized reversible universal shift register with the help of proposed Modified FRG1 and Modified FRG2 gates. We compare our design with existing ones in literature which claims our success in terms of number of gates, number of garbage outputs and delay. This optimization can contribute significantly in reversible logic community.

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