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Step-Wise Approximation Technique in the Design of a Function Generator

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ABSTRACT

In this work a simplified yet innovative approach was used to realize the digital function generator by adopting an analog device, a potential divider, to replace the Programmable Read Only Memory (PROM) stage and all its debacles, and a multiplexer to replace the Digital-to-Analog (DAC). The stepped voltage waveform obtained from the synthesis is passed through a low-pass filter (LPF) to achieve a high-purity sine wave. A corresponding 50% duty cycle square wave was obtained from the up-counter used for switching the multiplexer. This was integrated to generate triangular wave. The output stage provided impedance matching of 50Ω presented at a BNC output connector.

Keywords: *Multiplexer, Direct Digital Synthesis (DDS), Step-wise waveform, Function Generator, Impedance Matching.*

1. INTRODUCTION

The function generator as an electronic test equipment used for experimental measurement and test purposes generates various signal waveforms at different frequency ranges. The signal types range from the familiar sine wave, square wave, triangular wave and sawtooth wave to specialized wave functions like the modulation functions (AM, FM, ASK, FSK, etc), frequency sweeping functions, and other wave functions like ramp wave, unramped wave, arbitrary waves, TTL pulse, CMOS pulse, and so on.

Function generators came into use with the simulators used in analog computers in the mid-20th century [1]. In those designs, complex non-linear functions were realized as piecewise linear sections using electronic diodes. With rapid development of semi-conductors and monolithic circuits, large variety of designs have been developed leading to production of simpler, cheaper and accurate analog function generators. The most recent ones incorporate micro-controllers with specialized sampling and signal processing features [2]. With software realization that brought about digital concepts referred to as direct digital synthesis came state of the art designs that incorporate a standard set of hardware component blocks which include CPU, programmable memories and input/output interfaces to the analog world - the ADC and DAC [3].

The advantages of the digital function generators over the analog counterparts include higher frequency stability and accuracy, ability to generate much wider spectrum of standard and designer – specified programmable waveforms, with higher spectral purity, low phase noise and excellent frequency agility accompanying the use of digital filters that can be realized through software incorporated into the micro-controller.

The digital function generators fundamentally use digital to analogue converter (DAC) to generate wave shapes from values stored in memory. Digital synthesis of sine waves is employed in telephone line switching, modems and in many electronic instrument and telecommunication equipment. A variety of digital techniques are used of which the most versatile is the Direct Digital Synthesis (DDS).

2. THE DIRECT DIGITAL SYNTHESIS (DDS) TECHNIQUE

This technique convert digital numbers, which represent points that form the shape of a particular waveform, stored on a look-up table, into analogue or real signals. The look-up tables for different waveforms to be generated are stored in a Programmable Read Only Memory (PROM). DDS is a technology used in more advanced high-end function generators [4]. It generates a frequency- and phase-tunable output signal referenced to a fixed-frequency precision clock source.

The basic DDS consist of a numerically controlled oscillator (NCO) coupled with a phase modulator (or accumulator), a block that converts the phase information to amplitude values, and a digital-to-analogue converter (DAC) [5]. [6] indicated that the operation of DDS can be envisaged more easily by looking at the way a phase angle progresses over the course of one circle of a waveform as shown in figure 1. As the phase advances around the circle, this corresponds to advances in the waveform.

A signal is divided into 2^n data points on the phase wheel cycle in a complete cycle (360 degrees), with each data point rounded off to the nearest number. For n - bits of binary digits, all the number representing the signal and their phase increment are stored in the memory look-up table as shown in tables 1. A large number of points are required for each cycle of the waveform in order to achieve high spectral purity of the output signal.

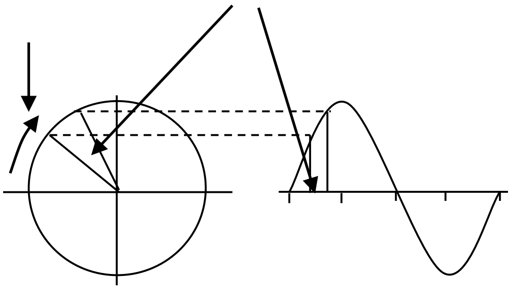

Figure 1: Phase progression around a circle in a DDS.

Table 1:Number of Points as a Function of Bit Length.

n	n - bits	No. of points	Phase increment value
8	8	256	360 / 256 = 1.40625
12	12	4096	360 / 4096 = 0.0878906
16	16	65535	360 / 65535 = 0.0054932
20	20	1048576	360 / 1048576 = 0.000343322
24	24	16777216	360 / 16777216 = 0.000021457
32	32	4294967296	360 / 4294967296 = 0.000000083
Etc			

The output frequency of a DDS device is determined by:

$$f_{out} = \{M(RefCLK)\}/2^n \text{ ………………………..…. (1)}$$

where, f_{out} is the output frequency, M is the binary tuning word, RefCLK is the internal reference clock frequency, and n is the length in bits of the phase accumulator.

3. THE DIRECT DIGITAL SYNTHESIS (DDS) FUNCTION GENERATION

Shown in figure 2 is block diagram of the basic DDS function generator. The DDS function generation has improved over the years with greater, wider frequency ranges, calibrated output levels, more variety of waveforms, modulation modes, computer interfacing and combination of sweeping or arbitrary functions. They offer substantial performance improvements, at reduced costs, over conventional analog function generators [7].

Data patterns for different signal waveforms stored in the EPROM are thereafter converted by the DAC to generate particular signal waveforms. For example, if the first half of the table for a signal pattern were filled with zeroes and the second half with values of 100%, then the data represent a square wave.

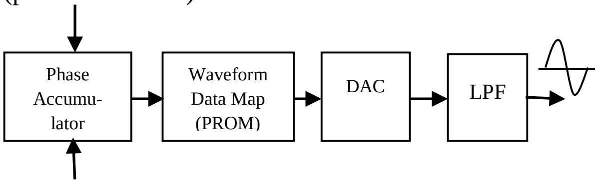

Figure 2: Block diagram of a basic DDS.

Advantages of the Direct Digital Synthesis (DDS) Function Generators include the following [8]

1. Micro-hertz frequency tuning of the output frequency and synthesized degree phase tuning capacity are possible under complete digital control.
2. A DDS generator can be swept over a much wider frequency range than an analogue generator.
3. Extremely fast "hopping speed" in tuning output frequency (or phase), phase - continuous frequency hops with no over/undershoot or analogue - related loop settling time anomalies.
4. The DDS digital architecture eliminates the need for the manual system tuning and tweaking associated with component aging and temperature drift in analogue synthesis solutions.
5. The digital control interface of the DDS architecture facilitates an environment where systems can be remotely controlled, and minutely optimized, under processor control.
6. When utilized as a quadrature synthesizer, DDS affords unparalleled matching and control of in-phase and quadrature (I&Q) synthesized outputs.
7. The DDS provides direct implementation of frequency, phase and amplitude modulation.

4. IMPLEMENTATION

The DDS signal generator was implemented for a sinusoid as the base signal for this function generator. The phase wheel in figure 1 was divided choosing n = 4 with the number of points on the wheel, $2^n = 16$ and the phase increment of the phase accumulator = $2\pi/16 = \pi/8$ (rad) or 360/16 = 22.5 (deg). The sine wave was synthesized in a step-wise pattern through the use of an array of resistors in a potential divider network to divide the +5 volts and ground into amplitudes according to the number of data points as shown in table 2 [9]. The sixteen values between 0 and 5 volts were provided as inputs to a sixteen input-channel analog multiplexer (CD4067BE) [10,11] to select through them for a complete cycle. Negative potentials were not used to avoid the multiplexer burning out and because it was easier to work with a single polarity power source. Switching through the sixteen input channels was enabled with the operation of a 4–bit Up-Counter (74LS93) [12], which was clocked with an oscillator circuit. The circuit connection is as shown in Fig. 3 and the stepped waveform at the output of the multiplexer is shown in Fig. 4. Since the amplitudes on the rise and on the fall side of the period are the same, so that the number of resistors used to produce the sixteen voltage steps was reduced to eight as seen in Fig. 3.

Table 2: Data Points and Steps Amplitude Values.

Data Point	Phase Angle (Rad)	Sine of Phase Angle	Stepped Amplitude (volts)	Values for Equal Step Amplitude
1	0	0	2.5	2.5
2	π/8	0.3827	3.4568	3.125
3	π/4	0.7071	4.2678	3.750
4	3π/8	0.9239	4.8098	4.375
5	π/2	1	5.0	5.000
6	5π/8	0.9239	4.8098	4.375
7	3π/4	0.7071	4.2678	3.750
8	7π/8	0.3827	3.4568	3.125
9	Π	0	2.5	2.5
10	9π/8	-0.3827	1.5433	1.875
11	5π/4	-0.7071	0.7322	1.250
12	11π/8	-0.9239	0.1903	0.625
13	3π/2	-1	0.0	0.0
14	13π/8	-0.9239	0.1903	0.625
15	7π/4	-0.7071	0.7322	1.250
16	15π/8	-0.3827	1.5433	1.875
1	2π	0	2.5	2.5

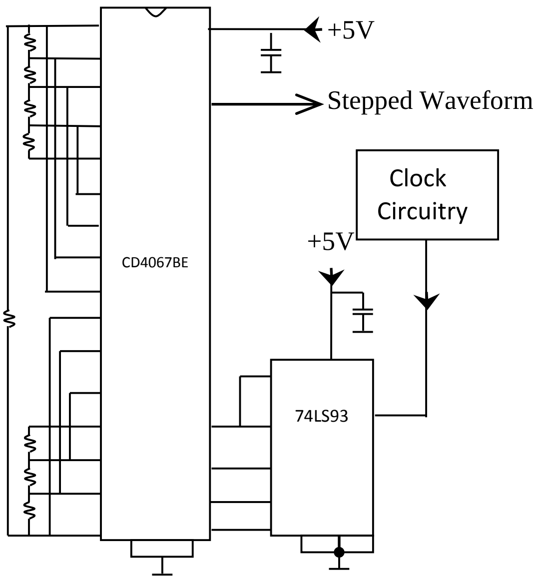

Figure 3: Circuit for realizing the Step waveform

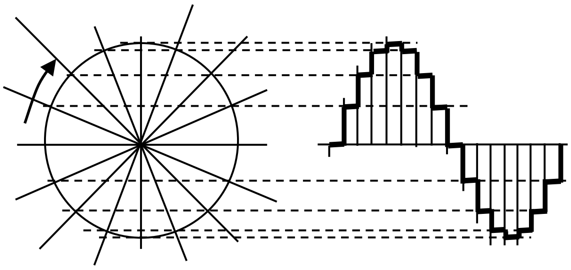

Figure 4: Step waveform from phase circle progression.

4.1 Equal Voltage Steps Approach

During experimentation, the unequal voltage step changes described above was realized. But the realization was clumsy, requiring resistors of various non-standard values to actualize the voltage steps. Subsequently, an approach of partitioning the whole value range into equal voltage steps was adopted so that same value resistors were used in the potential divider network [13]. This also allowed the use of R-R and R-2R ladder networks in the potential divider network, and the equal step values are as shown in column 5 of table 2.

4.2 Active Tuned RC Filter

The stepped voltage waveform obtained from the analog multiplexer was connected to a first order active Butterworth RC low–pass filter designed to obtain a clean low harmonic sine wave. The impedance of the RC filter network was obtained from:

$$Z = R \,||\, (\frac{1}{j\omega C})$$

$$= \frac{R/\,j\omega C}{R + 1/\,j\omega C} = \frac{R}{1 + j\omega RC} \quad \ldots\ldots\ldots\ldots(2)$$

With its magnitude given by:

$$|\,Z\,| = \frac{R}{\sqrt{1 + (\omega RC)^2}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(3)$$

The cut–off frequency of the filter network at 3-dB attenuation occurs at: $\omega_c RC = 1$. The filter was initially designed to allow passage of frequency signal up to the 3rd harmonic, which brings the allowed total harmonic distortion to about 1.13%.

The filter was developed from a normalized prototype [14] with a 3-dB normalized radian break frequency given as ϖ_0 = 1 rad/s and a d.c. gain of +1.

4.3 The Integrator Circuit

This circuit generates the triangular wave from the square wave obtained from the up-counter with the amplitude of the triangular wave given by:

$$V_o = -\frac{1}{RC} V_i t \text{ .... (4)}$$

$$= -\frac{V_i T}{\tau} = -\frac{V_i}{f\tau} \text{ .... (5)}$$

From equation (5) the frequency of the triangular wave increases as its amplitude decreases, that is, the amplitude of a triangular wave is inversely proportional to the frequency. To maintain steady or constant amplitude of the triangular wave, the time constant was made to vary in order as the frequency varies. This implied varying the values of resistance and capacitance (RC) that make up the time constant.

Making the time constant, τ the subject of the formula, equation (5) becomes:

$$\tau = RC = -\frac{V_i}{V_o f} = -\frac{K}{f} \text{ .... (6)}$$

where K is the ratio of the amplitude of the input signal to the amplitude of the triangular wave. K = 1 was chosen into the calculations so that the two amplitudes are relatively equal.

4.4 The Output Stage:

The selected generated signal goes into the final stage which is made up of an impedance matching buffer amplifier and a Symmetrical – T attenuator as shown in Fig. 5. These prevent deterioration of the output signal by the impedance of a load connected to it, making use of the impedance characteristics of an Op–Amp as a voltage follower, and of the attenuator network. With these impedance characteristics, there is virtually no interaction between the signal source and the load [15] and the possibility of "maximum power transfer" to the load or device connected to the function generator is guaranteed.

The attenuator network was designed for an attenuation of 10-dB at an output impedance of 50Ω. So that the attenuation or insertion loss is given by:

$$N = \frac{I_S}{I_L} = \frac{R + R_A + R_B}{R_B}$$

$$= \text{antilog of } 0.5 = 3.16 \text{ .... (7)}$$

where 20 log $\frac{I_S}{I_L}$ = 10-dB.

For impedance matching and maximum power transfer to occur is R, with which from analysis we arrived at the quadratic equation of R_A as follows:

$$(N+1)R_A^2 + R(2-N)R_A - R^2 = 0 \text{ .... (8)}$$

Solving this equation gives R_A = 33Ω and substituting into (7) gives R_B = 39Ω.

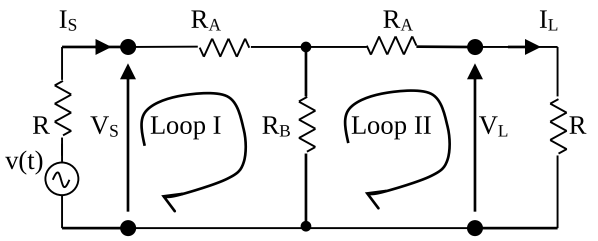

Figure 5: Symmetrical–T attenuator pad at Output stage.

5. OUTPUT WAVEFORMS

The output waveforms captured on an oscilloscope are shown in figures 6, 7, 8 and 9.

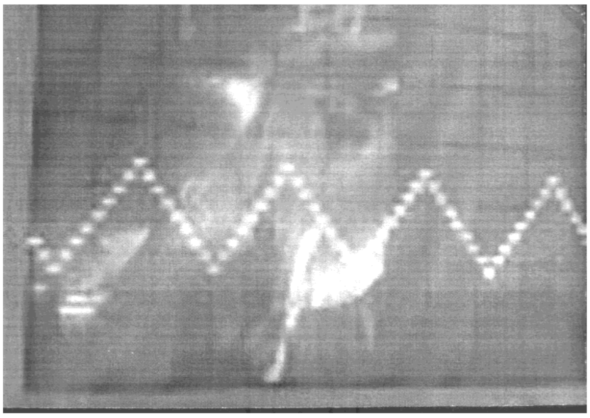

Figure 6: Test results – the stepped waveform.

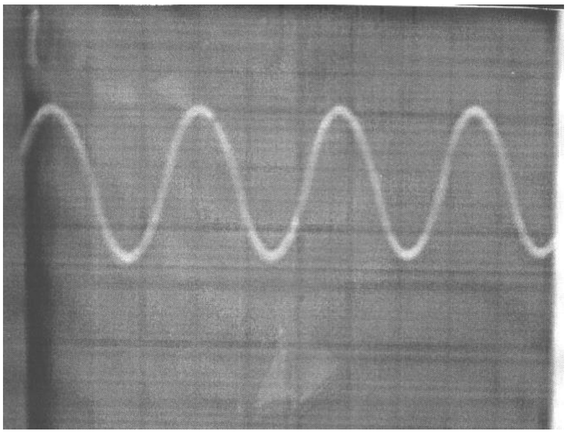

Figure 7: Test results – sinusoidal waveform

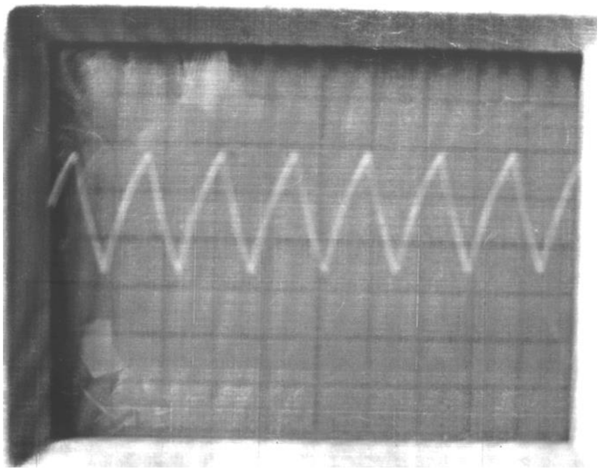

Figure 8: Test results – triangular waveform.

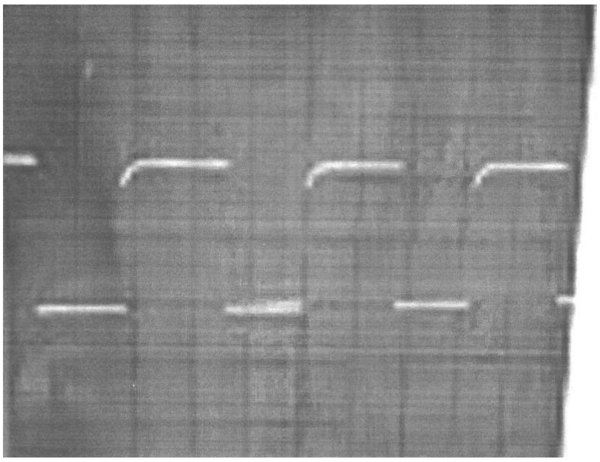

Figure 9: Test results – square wave

6. CONCLUSIONS

Function generator as an inevitable test equipment for use in laboratories in tertiary institutions and industry has, by this project, been analyzed, designed, prototyped and proved possible to locally mass produce it for teaching, research and practice in electrical and electronic engineering fields of specializations.

In fulfilling the objectives of this project, different types of function generators and different design techniques were studied. Simplicity, reliability and maintainability were observed in selecting the step-wise approximation technique for the design and construction of a 50Hz to 500kHz prototype function generator. These were also observed in the choice of components and in the approach for realizing the stages of the function generator.

Modular approach was adopted for the design of the stages of the prototype for ease of realization and troubleshooting. The overall design, construction and results obtained were satisfactory. Test waveforms were captured and printed out.

For future work it is recommended that R – 2R ladder network be used to replace the potential divider network entirely to reduce clumsiness and that higher order active filters be used to further improve on the response of the sine wave.

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