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Design of Reversible Multiplier by Novel ANU Gate

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ABSTRACT

In this paper, a novel Reversible logic gate has been proposed and novel architecture for multiplier is constructed by using proposed gate and Peres gate. For Partial Product Generation RSG Gate is used. This Multiplier gives better results when compared to previous circuits. This novel Gate can be used to design any Boolean logic expression and also any logic gate. The primary characteristics like garbage outputs, Constant inputs and number of gates got decreased. The logical calculations also got decreased. Power dissipation for Reversible logic gates is very less because of its reversibility property. So in present era, reversible logic gates can be used in many applications like bioinformatics, low power CMOS design, optical, quantum computing, DNA computing and also thermodynamic technology, Nanotechnology. The simulation was done in modelsim and synthesis was done by using rc compiler.

Keywords: *Reversible logic, Nanotechnology, Quantum computing.*

I. INTRODUCTION

In our present era decreasing power and increasing speed are two major concerns for any VLSI design. Normally in Irreversible gates there is no one to one mapping between the outputs and inputs and also power dissipation is also high and leakage of power is high. So we are going towards the new logic called the Reversible logic. According to R.Landauer, Irreversible gates can have more hardware complexity and high power dissipation because of information loss in the circuits[3,1]. In previous papers, information loss per bit can be given as KTln2 joules at least per bit where K is Boltzmann constant and the value is $1.3806505 \times 10^{-23}$ (J/K) and T is given as the absolute Temperature in Kelvin's[1]. At room temperature the amount heat dissipated is very small but it is not negligible it is approximately 2.9×10^{-21} Joules. The heat obtained from single bit is small but according to moore , heat dissipation can increase in exponential fashion. The logic which does not have any information losses are called as the Reversible logic's. All computations which are considered to be quantum are necessarily to be a Reversible. All logic gates like AND, NOR, NAND, OR, EXOR etc are not Reversible except NOT gate.

Reversible logic gates has many applications in many research fields such as bioinformatics, low power CMOS design, optical, quantum computing, DNA computing and also thermodynamic technology, Nanotechnology. Multiplication is one of the fundamental block in almost all the arithmetic logic units.

In this Paper, totally five sections are there. Section I explains about complete introduction related to the Reversible logic gates and second section II describes about basics of Reversible logic gate and also all fundamental definitions related to it. Section III describes about complete list of logic gates present till now and also basic fundamental Reversible logic gates. Section IV describes about proposed Reversible logic gate and its expressions and truth table and explanation for its functioning as full adder and proposed N-bit adder circuits and also proposed multiplier circuit. Section V describes about results and comparison of proposed architecture with all previous architectures.

II. BASICS OF REVERSIBLE LOGIC GATES

There are many number of reversible logic gates such as NOT gate, CNOT gate, FEYNMAN gate etc All the reversible gates can have certain properties needed to be satisfied and all the definitions and properties related to reversible logic gates are discussed in below sections.

A. Basic Definitions:

A KxK Reversible logic gate can be represented as below

$I_V = (I_1, I_2, I_3, I_4, I_5, \ldots\ldots\ldots I_k)$

$O_V = (O_1, O_2, O_3, O_4, O_5, \ldots\ldots\ldots O_k)$

where O_V and I_V represents output and input vectors.

1. *Reversible Function:*

A Function $F(y_1, y_2, y_3, y_4, \ldots\ldots y_n)$ with n number of output variables is said to be a reversible function if it satisfies the following conditions are

a. It has equal number of outputs and inputs.
b. The pre-image of the output pattern should be unique one i.e there should be one to one mapping between outputs and inputs[3,4,5].

2. *Reversible logic gate:*

A logic gate is said to be reversible if and only if

a. The number of inputs and number of outputs are equal to each other.
b. A one to one correspondence should present between inputs and outputs.

3. *Constant inputs[12]*:

These are one type of inputs which are unused in the design or to be kept as constant like 0 or 1 in the design so as to make it as Reversible. The total inputs are equal to the sum of the constant inputs plus primary inputs.

4. *Garbage outputs[8]:*

Garbage outputs are the extra outputs that are produced with in the design or the unused outputs are also called as the garbage outputs or in some cases the function can be a next function in order to make the function as reversible we can add some extra outputs are called as the Garbage outputs.

P.I + C.I = P.O + G.O.....(1)

where P.I represents primary inputs
C.I represents constant inputs
P.O represents primary outputs
G.O represents garbage outputs.

5. Quantum cost:

Quantum cost is defined as the cost of design in terms of the cost of primitive gates. It can also be stated as the number of primitive reversible logic gates needed to produce the complete design. There are two primary primitive gates are 1x1, 2x2 both have the cost of zero and one respectively.

Some of the design constraints of Reversible logic gates are given as below [8,4]

1. The number of fanouts should be zero.
2. Quantum cost should be minimum.
3. Garbage outputs should be minimum.
4. Constant inputs should be minimum.
5. Minimum complexity or less number of logic gates.

III. REVERSIBLE LOGIC GATES

At present, so many reversible logic gates are there some of the logic gates are discussed in this section. The primary basic reversible gates are 1x1 and 2x2 which have the cost of zero and one respectively. Each gate has different values of Quantum costs and Quantum cost can be calculated by counting the number of V+,CNOT and V gates. V is obtained by calculating the square root of the NOT gate and V+ is obtained by the Hermitian of V. Some of the properties are given below

V * V = NOT ..... (1)
V * V+ = V+ * V = 1 ..... (2)
V+ * V+ = NOT ..... (3)
Some of the fundamental Reversible logic gates are given as below

1) NOT Gate:

This is fundamental gate among all Reversible logic gates and quantum cost of this gate is zero and it is a1x1 reversible logic gate. The input and output vectors can be given as below
I_v=A and O_v = (X=A').

The truth table is shown in table1and block diagram in fig1shown as below

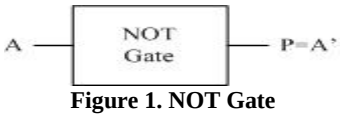

Figure 1. NOT Gate

Table 1. NOT Gate

A	P=A'
0	1
1	0

2) CNOT Gate :

This is also one of the fundamental gate and the cost is one and it is a 2x2 Reversible logic gate. The input vector and output vector are given as
I_v= (A,B) and O_v = (X=A,Y=A^B)

The truth table is shown in table2 and block diagram in fig2 shown as below

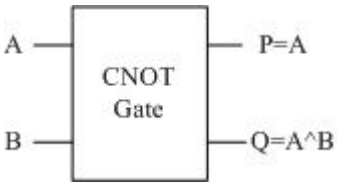

Figure 2. CNOT Gate

Table 2. CNOT Gate

A	B	P=A	Q=A^B
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

3) FEYNMAN Gate [6]:

It is also known as the copying gate or Controlled NOT gate(CNOT). It is a 2x2 Reversible logic gate and the Quantum cost is 1.

I_v= (A,B) and O_v = (X=A,Y=A^B)

The truth table is shown in table 3 and block diagram in fig3 shown as below

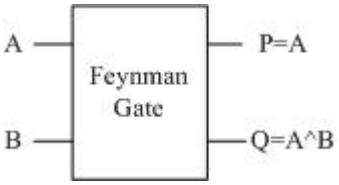

Figure 3. FEYMAN Gate

Table 3. FEYNMAN Gate

A	B	P=A	Q=A^B
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

4) Double Feynman Gate (F2G):

It is also called as Double Feynman gate and it is 3x3 reversible gate. The input vector and output vector are given as

I_v= (A,B,C) and O_v = (X=A,Y=A^B, Z=A^C)

The truth table is shown in table 4 and block diagram in fig4 as shown below

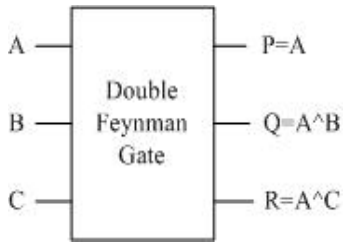

Figure 4. Double Feynman Gate

Table 4. Double Feynman Gate

A	B	C	P=A	Q=A^B	R=A^C
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

5) TOFFOLI Gate:

It is a 3x3Reversible logic gate and the Quantum cost is five. The input vector and output vector are given as

I_v= (A,B,C) and O_v = (X=A,Y=B, Z=A.B^C)

The truth table is shown in table 5 and block diagram in fig5 as shown below

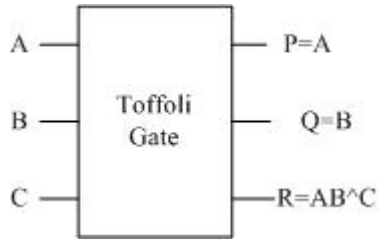

Figure 5. TOFFOLI Gate

Table 5. TOFFOLI Gate

A	B	C	P=A	Q=B	R=AB^C
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

6) FREDKIN Gate[15]:

It is a 3x3Reversible logic gate and the Quantum cost is five. This gate can be used as a 2x1 Multiplexer. The input vector and output vector are given as

I_v= (A,B,C) and O_v = (X=A,Y=A'.B+A.C, Z=A.B+A'.C)

The truth table is shown in table 6 and block diagram in fig 6 as shown below

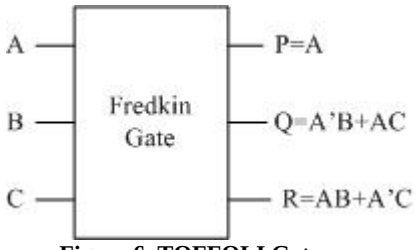

Figure 6. TOFFOLI Gate

Table 6. Fredkin Gate

A	B	C	P=A	Q=A'B+AC	R=AB+A'C
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

7) PERES Gate:(PG)[11]

It is a 3x3Reversible logic gate and the Quantum cost is four. This gate can be used as a half adder circuit. The input vector and output vector are given as
I_v= (A,B,C) and O_v = (X=A,Y=A^B, Z=A.B^C)

The truth table is shown in table 7 and block diagram in fig 7 as shown below

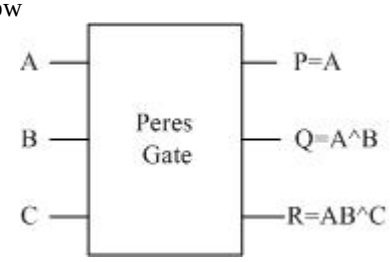

Figure 7. PERES Gate

Table 7. PERES Gate

A	B	C	P=A	Q=A^B	R=AB^C
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

7) RSG Gate:[29]

It is a 5x5 Reversible logic gate. This gate can be used for Partial Product Generation. The input vector and output vector are given as

I_v=(A,B,C,D,E) and O_v=(P=A, Q=B, R=C, S=A.B^D, T=A.C^E). The block diagram is shown below

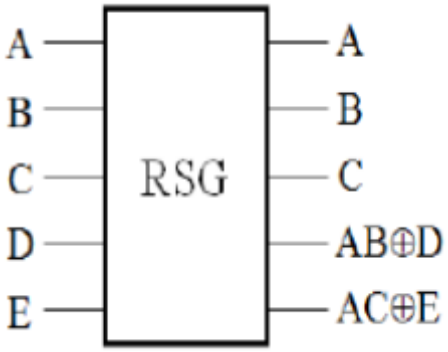

Figure 8:RSG gate

The delay and cost of fundamental Reversible logic gates are given in table 8.

Table 8. Delay and cost

Type of gate	Worst case delay	cost
Controlled-V	1	1
Controlled-V+	1	1
Feynman	1	1
peres	4	4
toffoli	4	4
fredkin	5	5

IV.PROPOSED REVERSIBLE LOGIC GATE

In this section a new gate called ANU gate was explained and it is 4x4 gates and it can be used for copying, Full Adder.

A) Proposed ANU Gate:

This is our new proposed 4x4 Reversible logic gate which can mainly function as a full adder circuit. The inputs and outputs to this gate are given below

I_v=(A,B,C,D) and O_v=(P=A,Q=B,R=(A^B^D), S=(A^B)&C^(A&B)^D)

The truth table and block diagram of BHA gate as shown below

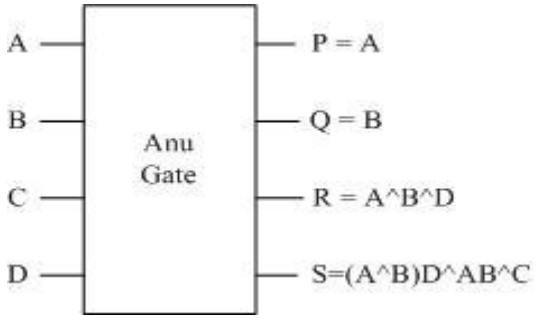

Figure 9.ANU gate

Table 9. Truth table for ANU gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	1
0	1	1	1	0	1	0	0
1	0	0	0	1	0	1	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	1	1
1	1	1	0	1	1	0	0
1	1	1	1	1	1	1	0

The input and output vectors for ANU Gate to function as a full adder was

I_v= (A,B,0,D) and O_v= (P=A,Q=B, R=Sum, S=Cout). The above ANU gate can have 1 constant input and 2 Garbage outputs.

The input and output vectors for ANU Gate to function as a full adder was

I_v= (A,B,0,0) and O_v= (P=A,Q=B, R=Sum, S=Cout). The above ANU gate can have 2 constant input and 2 Garbage outputs.

Let us consider
a= 2 input EXOR Gate
b= 2 input AND Gate
c= NOT gate
T= Total Logical Calculations

From [5]: T=6a+3b+3c, for [16]: T=5a+3b+3c and for this Proposed one T=5a+2b for each ANU gate. Hence the proposed full adder is better when compared to [5, 16].

B) ADDER Circuits:

Adders are the basic fundamental unit in any Arithmetic and logic unit. Ripple carry adders are the simplest architectures among all the types of adders. In ripple carry adder circuits carry is forwarded to the next stages and sum is generated at each stages.

1) Proposed Ripple Carry Adder circuit:
Let us consider a.b.c are the inputs to the gate and the sum can be given as the Si and Ci+1.The intermediate carry can be

forwarded o the next stages and at each stage the sum is generated and it is passed to the output stage. For each gate the number of garbage outputs are given as 2 and number of constant inputs are 1. Hence for a N-bit Ripple Carry Adder, generalized equation for Quantum cost can be given as (2G+1C)*N.
where N is the number of ANU gates used for N-bit adder.
The architecture for this ripple carry adder was given below.

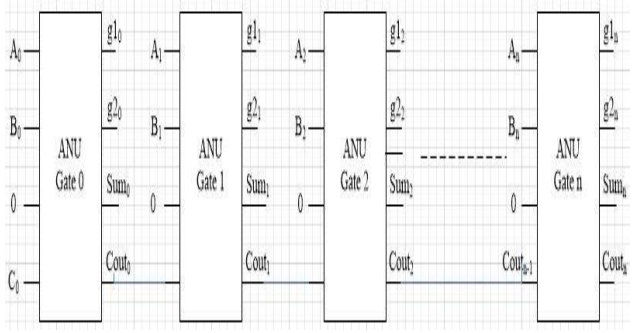

Figure 10. N-bit Ripple Carry Adder

C) Reversible Multiplier using ANU Gate:

In this section, a proposed architecture for 4x4 multiplier was shown in figure 12. To implement any multiplier we need adders and the adders for that multiplication has been produced by using ANU gate as mentioned above. Here for implementing a multiplier we have 2 steps are

1) Partial Product generation
2) Addition of Partial products

Here in this paper Partial product generation can be done by using RSG Gate because of its less Quantum cost and less complexity in hardware. Totally to implement a complete 4x4 multiplier we need 8 BHA, 8 RSG Gates and 4 PERES gates. For Partial Product generation we need 8 BME Gates and for each RSG Gate has 3 Garbage outputs and 2 Constant input and for each ANU Gate has 1 Constant input and 2 Garbage outputs. For this proposed ANU gate has Total logical calculation of T=64a+36b+0c and for [20] the Total logical calculation is: T=110a+103b+71c, and for [22] the logical calculation is:T=80a+100b+68c, for [21] the Total logical calculation is: T=92a+52b+36c . Hence proposed circuit is better than [20-22]. The multiplier partial products has shown in below figure11

The Partial products can be generated by using RSG Gate
Is shown in below figure11.

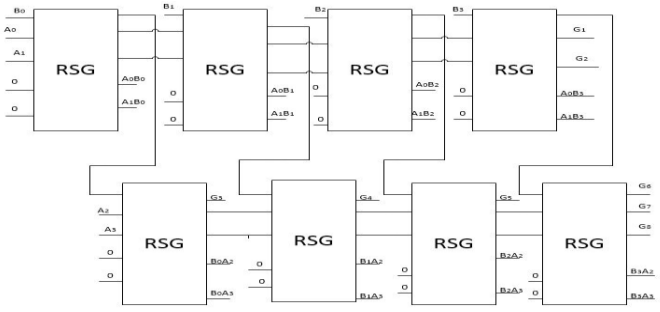

Figure 11: Partial Product Generation using RSG Gate.

Table 10. Comparison of different Partial Product Generations.

PARTIAL PRODUCT GENERATION	NO:Of GATES	NO:OF C.I	NO:OF G.O	QUANTUM COST(QC)
PROPOSED	**8**	**16**	**8**	**40**
PG[25]	28	40	32	88
MKG[2]	40	40	32	88
PFAG[12]	40	40	32	88
HNG[9]	40	40	32	88
TSG[4]	40	40	32	104

The Proposed architecture for 4x4 multiplier has shown in below Figure 12.

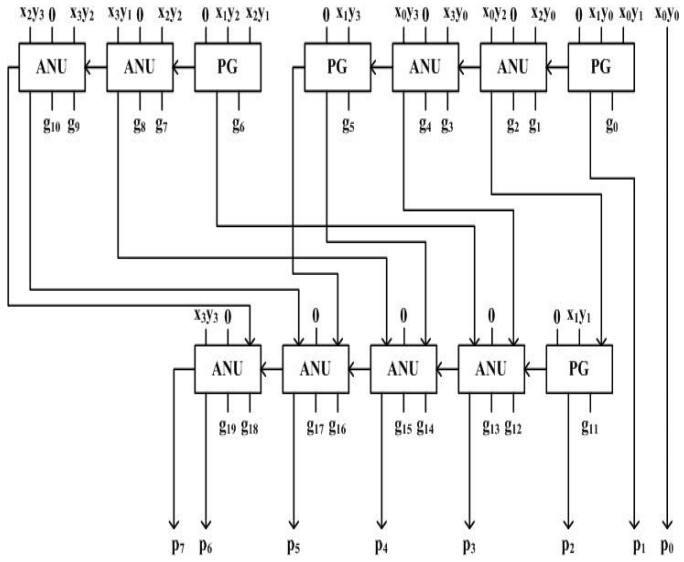

Figure 12. Proposed architecture for 4x4 Reversible multiplier using ANU and PERES Gate.

In the above architecture we have mainly used 8 Full adders and 4 Half adder circuits. The ANU Gate can be used as a Full adder circuit and PERES gate can be used as Half adder and also partial products generation. For Partial Product generation we use PERES Gate because of this one hardware complexity gets decreased when compared to the [20-27]. The comparison table of different Reversible multipliers has shown in below Table 11.

Table 11. Comparison of different Reversible multiplier results.

REVERSIBLE MULTIPLIER	NO:OF GATES	NO:OF C.I	NO:OF G.O
PROPOSED MULTIPLIER	**20**	**28**	**28**
[27]	28	28	22
[24]	28	28	32
[23]	28	28	28
[22]	28	28	52
[21]	28	32	56
[20]	29	34	58
[19]	40	31	56
[25]	40	52	52
[2]	52	56	56
[12]	52	52	52
[9]	52	52	52
[4]	53	58	58

IV. RESULTS AND DISCUSSION

In this paper mainly we have compared three parameters of reversible gates are the number of Reversible logic Gates, number of Garbage outputs, number of Constant inputs and also Total number of logic calculations. Here the Proposed circuit is better in all fields and give better results.

Garbage outputs are the outputs other than the primary outputs and in this paper its count is 28 far better than previous papers [20,21,22].

Constant inputs are also very less when compared with previous paper work [20,21,22]. Reversible gate count was slightly less than that of [21,22].

Total logical calculations are slightly got decreased i.e for this architecture it is T=64a+36b+0c. and for [20] it is T=92a+52b+36c and for [21] it is T=110a+103b+71c and for [22] it is T=80a+100b+68c.

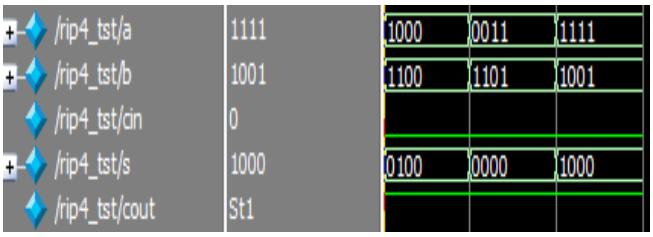

Figure 13. 4 bit adder using ANU gate

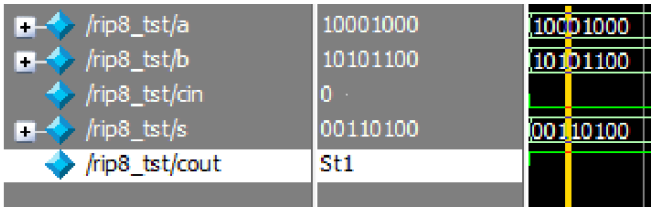

Figure 14. 8 bit adder using ANU gate

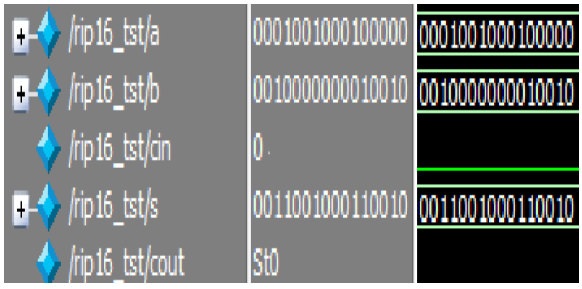

Figure 15. 16 bit adder using ANU gate

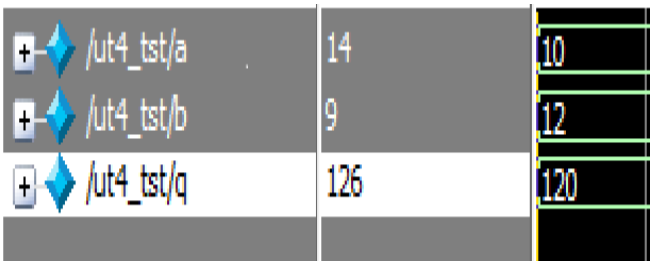

Figure 16. 4 bit multiplier using ANU gate

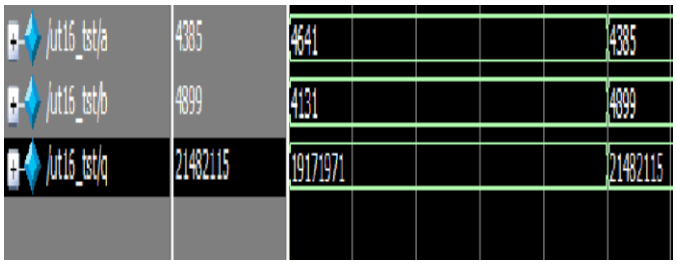

Figure 17. 16 bit multiplier using ANU gate

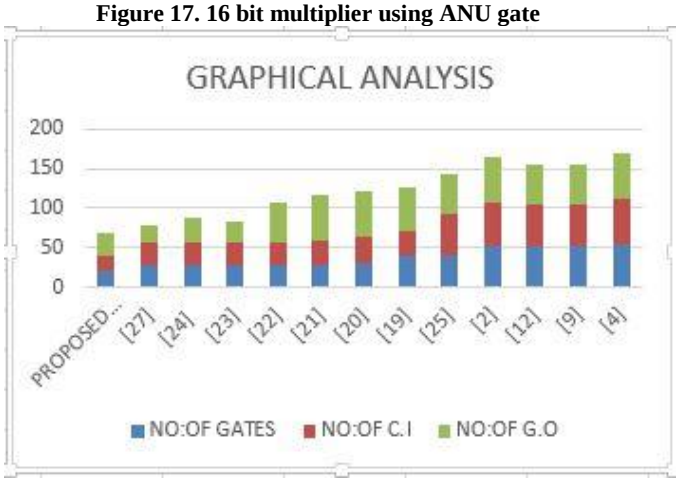

Figure 18. Graphical analysis of characteristics

V. CONCLUSION

The proposed multiplier gives better results when compared to other multiplier techniques because the number of logic calculations gets reduced by using ANU Gate and PERES Gate. The comparison results shows that the Garbage outputs and constant inputs got decreased and he number logical calculations also got decreased by this proposed multiplier. The Proposed multiplier is very useful in many applications in bioinformatics, low power CMOS design, optical, quantum computing, DNA computing and also thermodynamic technology, Nanotechnology.

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